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**1.1 System Monitor Introduction**

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Much of the machinery throughout the APS will be controlled by VME based computers. In order to increase the reliability of the system, it is necessary to be able to monitor the status of each VME crate. In order to do this, a VME System Monitor was created. In addition to being able to monitor and report the status (watchdog timer, temperature, CPU (Motorola MVME 167) state (status, run, fail), and the power supply), it includes provisions to remotely reset the CPU and VME crate, digital I/O, and parts of the transition module (serial port and ethernet connector) so that the Motorola MVME 712 is not needed. The standard VME interface was modified on the System Monitor so that in conjunction with the Motorola MVME 167 a message based VXI interrupt handler could be implemented.

The System Monitor is a single VME card (6U). It utilizes both the front panel and the P2 connector for I/O. The front panel contains a temperature monitor, watchdog status LED, 4 general status LEDs, input for a TTL interrupt, 8 binary inputs (24 volt, 5 volt, and dry contact sense), 4 binary outputs (dry contact, TTL, and 100 mA), serial port (electrical RS-232 or fiber optic), ethernet transceiver (10 BASE-FO or AUI), and a status link to neighbor crates. The P2 connector is used to provide the serial port and ethernet to the processor. In order to abort and read the status of the CPU, a jumper cable must be connected between the CPU and the System Monitor.

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**1.2 System Monitor Theory of Operation**

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The System Monitor consists of basically four sections; a VME interface which allows the reading and writing of the board functions, a status link which connects to neighboring crates using a serial fiber optic link, a serial port which allows for a CPU abort and a

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VME reset, and the physical connections for the console serial port and the ethernet.

### 1.2.1 VME Interface

The VME interface on the System Monitor was created by Bob Laird (1993). Added to this interface is the ability to capture 16 bit interrupt vectors. The MVME 167 is only able to latch the lower 8 bits of an interrupt vector, so this card expands the capabilities of the processor. When an interrupt is generated, the System Monitor will capture the presented 16 bit interrupt vector. This vector can then be recovered from the System Monitor board by reading functions 25 - 31, which correspond to IRQ1 - IRQ7 respectively.

The interrupt vector which the System Monitor can generate from any one of its binary inputs, is stored at the function 23 memory location.

In order to make the MVME 167 compatible with VXI message based interrupts, it was necessary to create a module which sits at memory location 0xC008. This module contains, in essence, a full VME interface. When the memory location 0xC008 is written to, the message is captured, and an interrupt is generated. This vector is controlled by function 24. The MVME 167 can then read back the message word, which is stored at location 0xC008.

The System Monitor essentially sits at two memory locations on the VME bus. The VME interface is configured to any valid memory location, but the VXI message based interrupter is hardwired to sit at 0xC000, function 4 (0xC008).

If the VXI message based interrupts are not going to be used, then it is not necessary to include some of the circuitry on the System Monitor. VME PLD B (U41), VME INTERRUPTER B (U42), and CONTROL REGISTER AND INT VECTOR (U43) are not necessary. If these PLDs are taken out, then it is necessary to insert JP26, JP27, JP28, and JP29, J8 and J9 should be removed. This will bypass all of the critical signals which these ICs would normally supply.

## 1.3 Status Link / Character Detector

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The status link is used to both transmit basic status information to a neighboring VME crate and to receive this information from a neighboring crate. This status includes the state of the watchdog timer, temperature, CPU status, CPU run status, voltage (both +12V/-12V and +5V), and the CPU fail status. The physical link is implemented with fiber optics based upon the serial port standard (9600, 1 start bit, 7 data bits, no parity). The status information is located at function 18. The received status is the lower order byte, and the status to be sent out can be monitored on the higher order byte.

The character detector monitors the console serial port for a specific sequence of characters. A Control-X should normally reset the VxWorks Software. Occasionally the CPU will "hang" and without this character detector, it would be necessary to physically go out to the crate and manually reset it. With the System Monitor Board, sending a Control-X followed immediately (within 500 mS) by a Control-Y will abort the CPU. If this still does not clear up the problem, a Control-X followed by a Control-Y and a Control-Z (this sequence must be completed in 1 S) will reset the VME backplane.

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A jumper cable (J5) must be installed between the MVME 167 and the System Monitor in order to take advantage of the remote monitoring of the CPU statuses and the CPU abort signal.

## 1.4 Digital I/O

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The System Monitor has four digital outputs and 8 digital inputs (P3). The outputs are current limiting solid state relays (120 mA) and can be either TTL, dry contact, or 100 mA. This is determined by the configuration jumpers (JP1 - JP4, JP21-24). The binary inputs can be configured for 12V-28V inputs, 5V-10V inputs, and dry contact sense using jumpers JP5 - JP20. The binary outputs are located in the lower order nibble of function 19. The binary inputs are located in the high order byte of function 19.

Ton and Toff for the Binary Outputs has a maximum value of 5 mS.

In addition the binary inputs can also be used to interrupt the VME backplane. These interrupts are maskable, and the mask is the low order byte of function 20.

Located on the front panel is a TTL input which is also a maskable interrupt. The mask for this bit is the least significant bit of the high order byte of function 20.

JP30 determines if the fourth digital output echoes that status of the OUT3 bit or the status of the watchdog timer. Echoing the status of the watchdog timer allows an external system, such as an Allen-Bradley Binary Input Module to monitor the watchdog status of the CPU.

## 1.5 Temperature Monitor

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The sensor used is a three pin (TO-92 package) device (U2) which can be mounted anywhere in the crate. There is a place on top of the board for this sensor so that it can measure the temperature of the air after it has been blown over the crate. This temperature is then displayed on the front panel using LEDs. The temperature can also be read back in the lower order byte of function 21. JP25 is used to configure the TEMP\_OK level which is passed on to the status link. The range which can be measured is from 20° C to 65° C in 5° C steps.

## 1.6 Voltage Monitor / Watchdog Timer

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Both the +12 Volt and the -12 Volt supply are monitored for under voltage. The +5 Volt supply is monitored for both over and under voltage. The statuses are fed to the Status Link. The +12 Volt and -12 Volt can fall by about 10% before the comparator trips, and the +5 Volt supply is monitored to about +0.1 Volt and - 0.4 Volt. [In working with the prototype, a problem was discovered, and the +5V checking was disabled on all production boards.]

The watchdog is triggered by a read function to the board. The board must be read from every 1.6 seconds or the watchdog will time out. This status is echoed to the Status Monitor as well as the front panel. There is a bi-colored LED on the front panel, green indicates that the CPU is polling the System Monitor, and red indicates that the CPU has stopped.

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In addition to a watchdog timer, this function also contains a latch, whose status is echoed by four front panel LEDs (yellow). The LEDs echo the bits in the lower order nibble of function 22. One possible use for these LEDs is to indicate the boot status of the CPU.

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## 1.7 Serial Port

Rather than use the MVME 712 transition module to break out the console serial port, it was decided that it would be put on the front panel of the System Monitor. It is designed to be a daughter board so that it could either implement electrical RS-232 or a standard fiber optic protocol. The advantage of this scheme is that the fiber optic serial port will be used throughout the APS because of its immunity to electrical noise and at least 1 KM distance limitation, while standard RS-232 will be used for test and development in the laboratory setting.

It is assumed that the console port will be set to the default configuration of 9600 baud, 1 start bit, 8 data bits, and no parity (9600,1,8,N). This default configuration is hard wired into the part of the circuit which monitors the serial port in order to detect a reset sequence.

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## 1.8 Ethernet Port

Like the serial port, to avoid the need for the transition module, an ethernet connector would be included on the front panel. It was decided that initially only an AUI connector would be offered on a daughter board. This would allow the board to stay compatible with future ethernet implementations.

It is hoped that the size of this daughterboard would allow other ethernet interfaces to be designed and easily installed, such as a 10-BASEFO interface.

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## 1.9 P2

The P2 connector is used to connect the console and ethernet ports on the System Monitor to the MVME 167. Since only rows A and C are necessary for this, a simple 64 pin mass terminated jumper cable can be used to connect the System Monitor to the MVME 167.

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## 1.10 Function Map of the System Monitor

The System Monitor utilizes functions 18 - 31. These functions were chosen so that future integration of the System Monitor with the APS Event Receiver would be easier to implement.

**TABLE 1.****FUNCTION DESCRIPTION**

<b>Function #</b>	<b>Address (0x8B80)</b>	<b>Function Name</b>	<b>Name</b>	<b>Description</b>
18 (LSB)	0x8BA4	Status Link RX	rWATCHDOG_OK (lsb) rnTEMP_OK rnSTAT rnRUN r+-12_OK r5_OK rnFAIL START_BIT	Watchdog status - bit 0 Temperature status - bit 1 CPU status - bit 2 CPU running status - bit 3 +- 12 Volts OK - bit 4 5 Volts OK - bit 5 CPU failure - bit 6 Undefined - bit 7
18 (MSB)	0x8BA5	Status Link TX	WATCHDOG_OK nTEMP_OK nSTAT nRUN +-12_OK 5_OK nFAIL START_BIT (msb)	Watchdog status - bit 8 Temperature status - bit 9 CPU status - bit 10 CPU running status - bit 11 +-12 Volts OK - bit 12 5 Volts OK - bit 13 CPU failure - bit 14 Undefined - bit 15
19 (LSB)	0x8BA6	Digital Output	OUTPUT[0..3] (reserved bits[4..7])	Dry Contact, TTL, 100mA
19 (MSB)	0x8BA7	Digital Input	INPUT[0..7]	Dry Contact, 5V-28V
20	0x8BA8 0x8BA9	Interrupt Mask	INPUT[0..6], TTL INPUT, (reserved bits[8..15])	Inputs to generate a VME interrupt
21	0x8BAA 0x8BAB	Temp Monitor	20 C - 65 C bits[0..7], (reserved bits[8..15])	This is a bar graph where each bit represents 5 C.
22	0x8BAC 0x8BAD	Watchdog	LED[0..3], Automatic_Reset[7], (reserved bits[4..6, 8..15])	Front panel LEDs to show boot status, and enable bit for automatic reboot on watchdog time-out.
23	0x8BAE	0xC008 Int Vector	DB[0..15]	Vector presented when location 0xC008 is written to, (capture of VXI)
24	0x8BB0	VME Int Vector	DB[0..15]	VME interrupt vector, user defined
25	0x8BB2	IRQ 1 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector
26	0x8BB4	IRQ 2 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector
27	0x8BB6	IRQ 3 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector
28	0x8BB8	IRQ 4 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector
29	0x8BBA	IRQ 5 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector
30	0x8BBC	IRQ 6 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector
31	0x8BBE	IRQ 7 Vector	DB[0..15]	Captured 16 bit VXI IRQ1 Vector

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## 1.11 Configuration

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### 1.11.1 JP1 - JP4, JP21 - JP24 : Digital Output

JP1, JP3, JP21, and JP23 are installed when the output is to be TTL or 100 mA.  
JP2, JP4, JP22, and JP24 are installed when the output is to be TTL.  
No jumpers are inserted for a Dry Contact output.

A Dry Contact output is connected between OUT+ and OUT-.  
A TTL or 100 mA output is connected between OUT- and GROUND.

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**TABLE 2.**

Digital Output Configuration

JP[1, 3, 21, 23]	JP[2, 4, 22, 24]	CONFIGURATION
IN	IN	TTL (OUT-, GROUND)
IN	OUT	100 mA (OUT-, GROUND)
OUT	OUT	Dry Contact Sense (OUT+, OUT-)

### 1.11.2 JP30 : Watchdog Output

This jumper is used to determine if the value of OUT3 is generated from the state of the watchdog timer or from the boards register.

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**TABLE 3.**

OUT3 Configuration

JP30	CONFIGURATION
1-2 (Top)	nWatchdog Status
3-4 (Bottom)	Register OUT3

### 1.11.3 JP5 - JP20 : Digital Input

All of the jumpers are removed for a 12V - 28V input, between IN+ and IN-.  
JP5, JP7, JP9 ... JP19 (JP A) are inserted for a 5V - 10V input, between IN+ and IN-.  
JP6, JP8, JP10 ... JP20 (JP B) are inserted for a Dry Contact Sense input, between IN- and GROUND.

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**TABLE 4.**

Digital Input Configuration

JP A	JP B	CONFIGURATION
OUT	OUT	12V - 28V input (IN+, IN-)
IN	OUT	5V - 10V input (IN+, IN-)
OUT	IN	Dry Contact Sense (IN-, GROUND)

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#### 1.11.4 J6 - J9 : Interrupt Level

These jumpers determine which interrupt request level is used by the corresponding VME module. JP6 and JP7 are for the System Monitor IRQ level. JP8 and JP9 determine which level the VXI message based interrupt generates.

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**TABLE 5.** Jumpers J6 and J8

Pins 1-2	Pins 3-4	...	Pins 11-12	Pins 13-14	INT Level
OUT	OUT	OUT	OUT	OUT	DISABLED
IN	OUT	OUT	OUT	OUT	1
OUT	IN	OUT	OUT	OUT	2
OUT	OUT	...	OUT	OU	[3..5]
OUT	OUT	OUT	IN	OUT	6
OUT	OUT	OUT	OUT	IN	7

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**TABLE 6.** Jumpers J7 and J9

Pins 1-2	Pins 3-4	Pins 5-6	INT Level
IN	IN	IN	0
OUT	IN	IN	1
IN	OUT	IN	2
...	...	...	...
IN	OUT	OUT	6
OUT	OUT	OUT	7

#### 1.11.5 JP25 : Temperature Monitor

This determines the set point at which the nTEMP\_OK signal is set. This level can range from 20° C (pins 19-20) to 65° C (pins 1-2) in 5° C increments.

#### 1.11.6 JP26 - JP29 : VXI Message Based Interrupt

When these jumpers are installed, the VXI Message based interrupt handler will be disabled on the System Monitor. These jumpers should also be installed if the VME\_PLD\_B (U41), VME\_INTERRUPTER\_B (U42), and INT (U43) are not present on the board.

**FIGURE 1**

**Configuration Jumper Placement on the System Monitor Board**

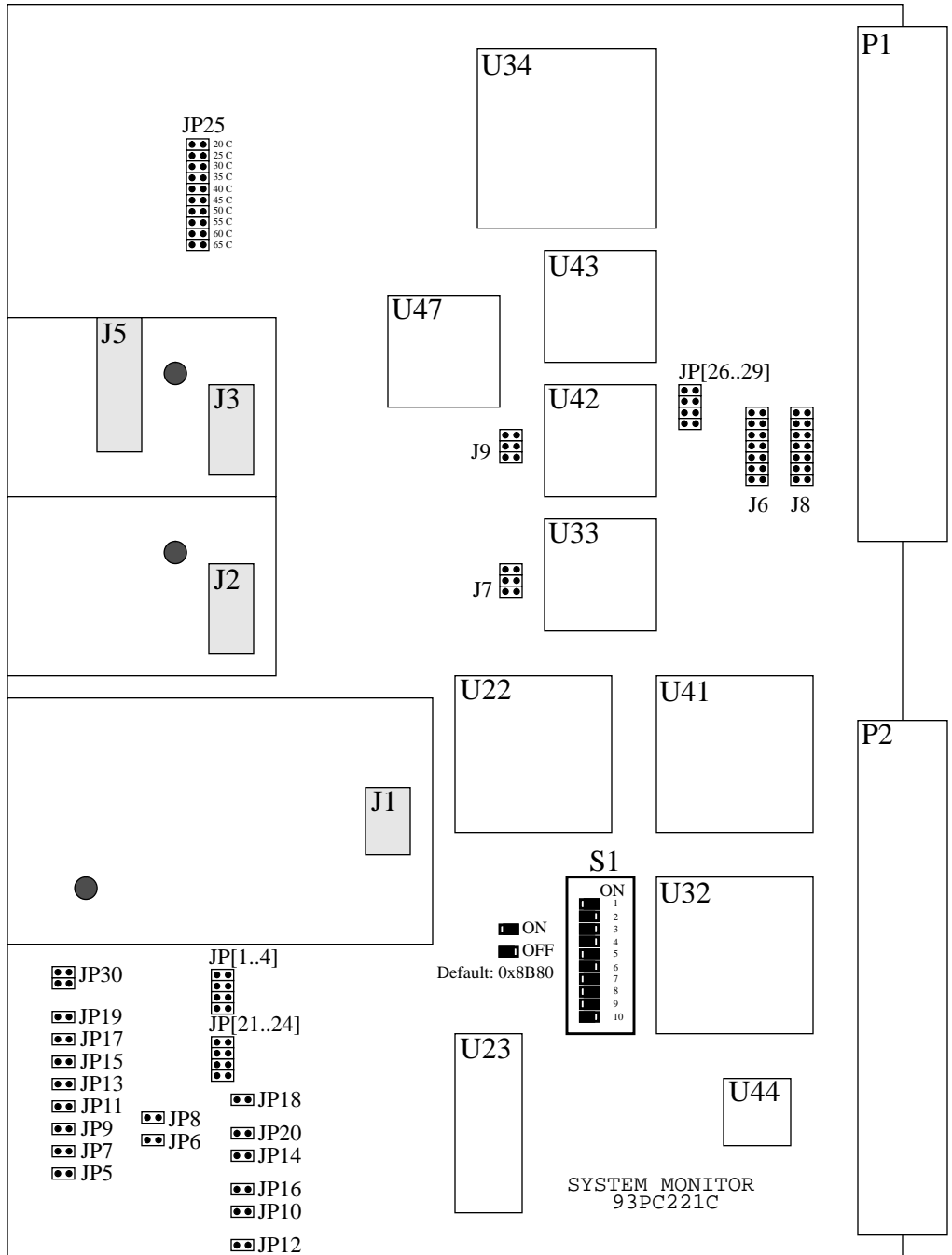
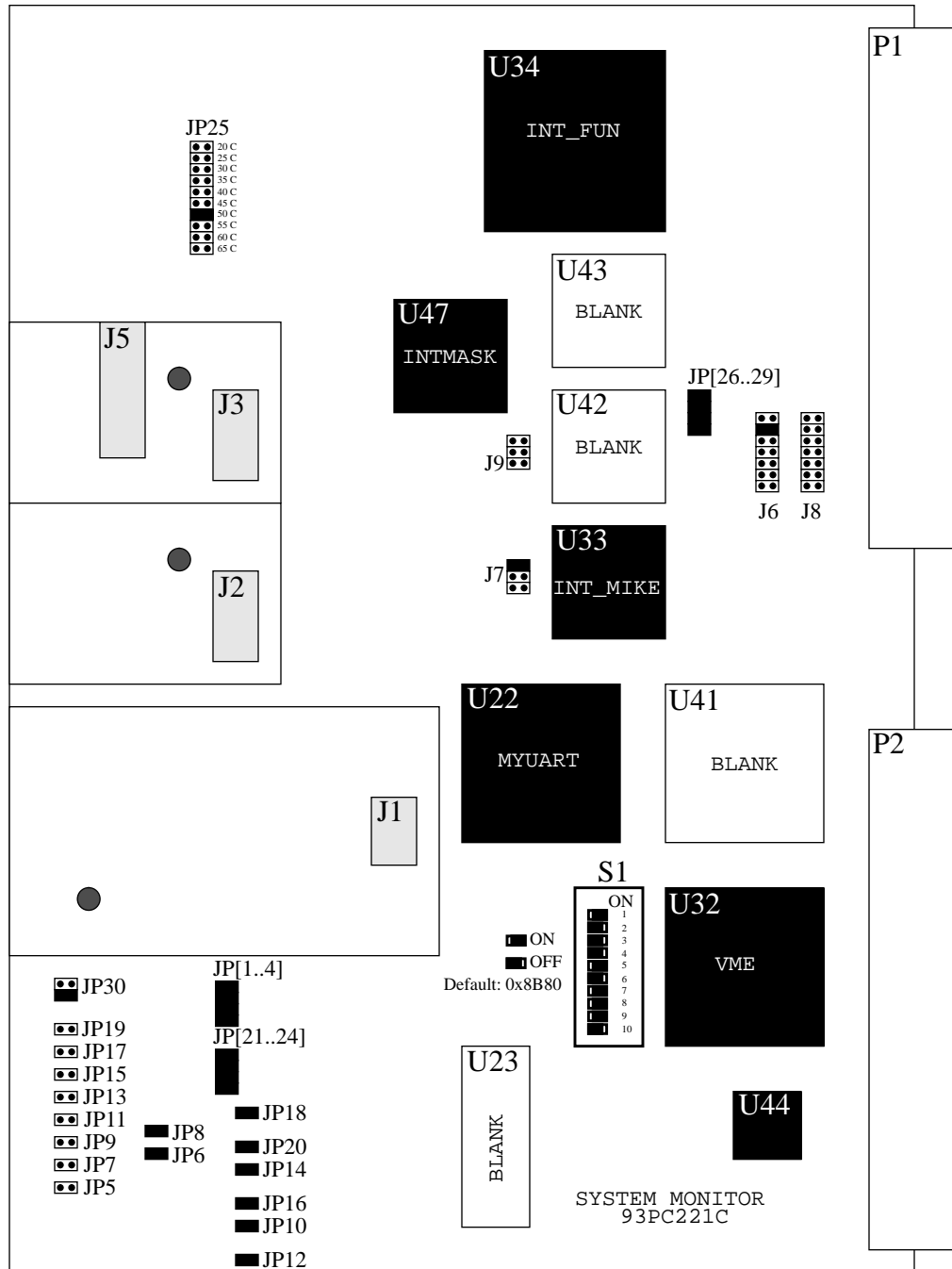




FIGURE 2

Default Configuration of System Monitor Board



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## 1.12 System Monitor Assembly

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The System Monitor is a standard VME (6U) card. If the status of the processor is to be monitored by the card, it is necessary that the card be placed in the slot adjacent to the processor. There is a short ribbon cable which attaches the two card. Due to the placement of the connector on the MVME-167, it was necessary to place the corresponding connector on the System monitor board in the same position, by the front panel. The ribbon cable is to be run between the circuit board and the front panel. Once the cable is in place, it will be necessary to take out both boards together if either one needs to be serviced.

The Ethernet and serial connection between the System Monitor and the processor utilize the P2 connector on the VME backplane. The A and C rows of each board's P2 connector must be connected together. This can be done using mass terminated 64 pin ribbon cable. This cable is then installed on the rear of the VME crate.

The completed System Monitor Board will contain three daughter boards. One is for the Ethernet connection. In the first version this will just be an AUI connector, the signals from the AUI connector are essentially jumpered from the front panel of the System Monitor to the P2 of the MVME-167.

Another daughter board is for the console serial port. This daughter board will either be an electrical or fiber optic RS-232 transceiver. The two options are offered so that in the laboratory setting the standard (and convenient) electrical interface can be used, and when the boards are installed in the Advanced Photon Source the noise immune fiber optic interface can be used. The transceiver converts the incoming serial signal to TTL levels so that it can be monitored for the reset sequence and then back to RS-232A levels for use by the processor.

The third daughter board is used for the status link between the boards. The circuitry on this board is identical to that on fiber optic transceiver board, except that the MAX233 chip is omitted and pins 19 and 20 are jumpered. This third daughter board was created to make room for cable which supplies the status information from the CPU to the System Monitor.

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## 1.13 Device Support

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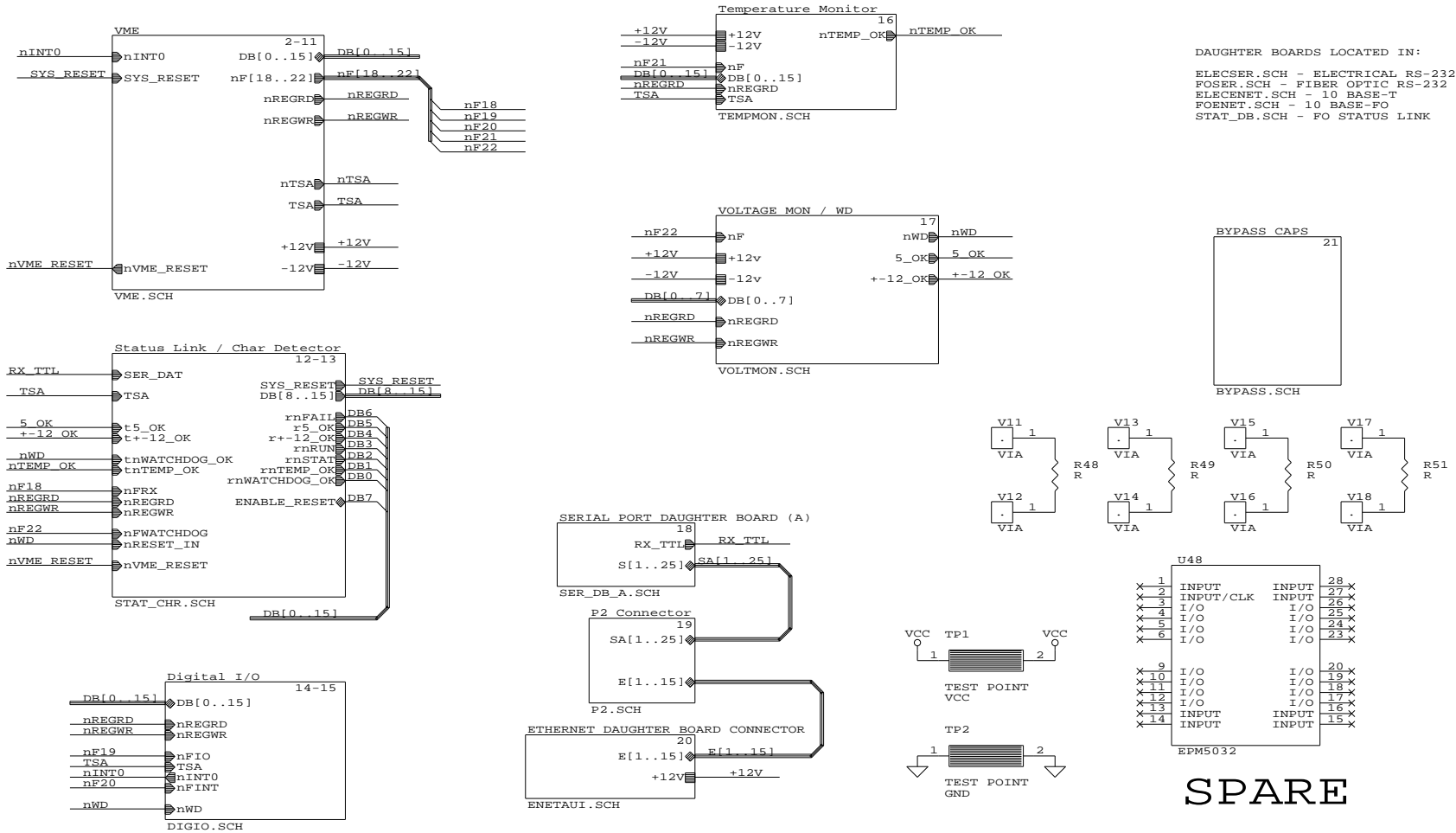
The System Monitor Board supports Binary Output (BO), Binary Inputs (BI), Analog Inputs (AI), MultiBit Binary Output (MBBO), and MultiBit Binary Input (MBBI). When defining a Process Variable, one should choose the "SYSMON" device option. The card number indicates which System Monitor Board you are accessing in a particular crate (typically this field will be equal to 0, up to two cards are supported, 0 and 1). The signal field acts as a mask so that you can specify which bit you are accessing with a BO or a BI. The following line must be executed at startup in order to initialize the System Monitor Board:

```
SysmonConfig(card #, A16 address, VME int vector, VME int level, VXI int vector)
SysmonConfig(0, 0x8b80, 0x71, 0x6, 0x72)
```

The Parameter field then contains the name of the register you want to access:

**TABLE 7.** Device Support Parameter Field Entry Options

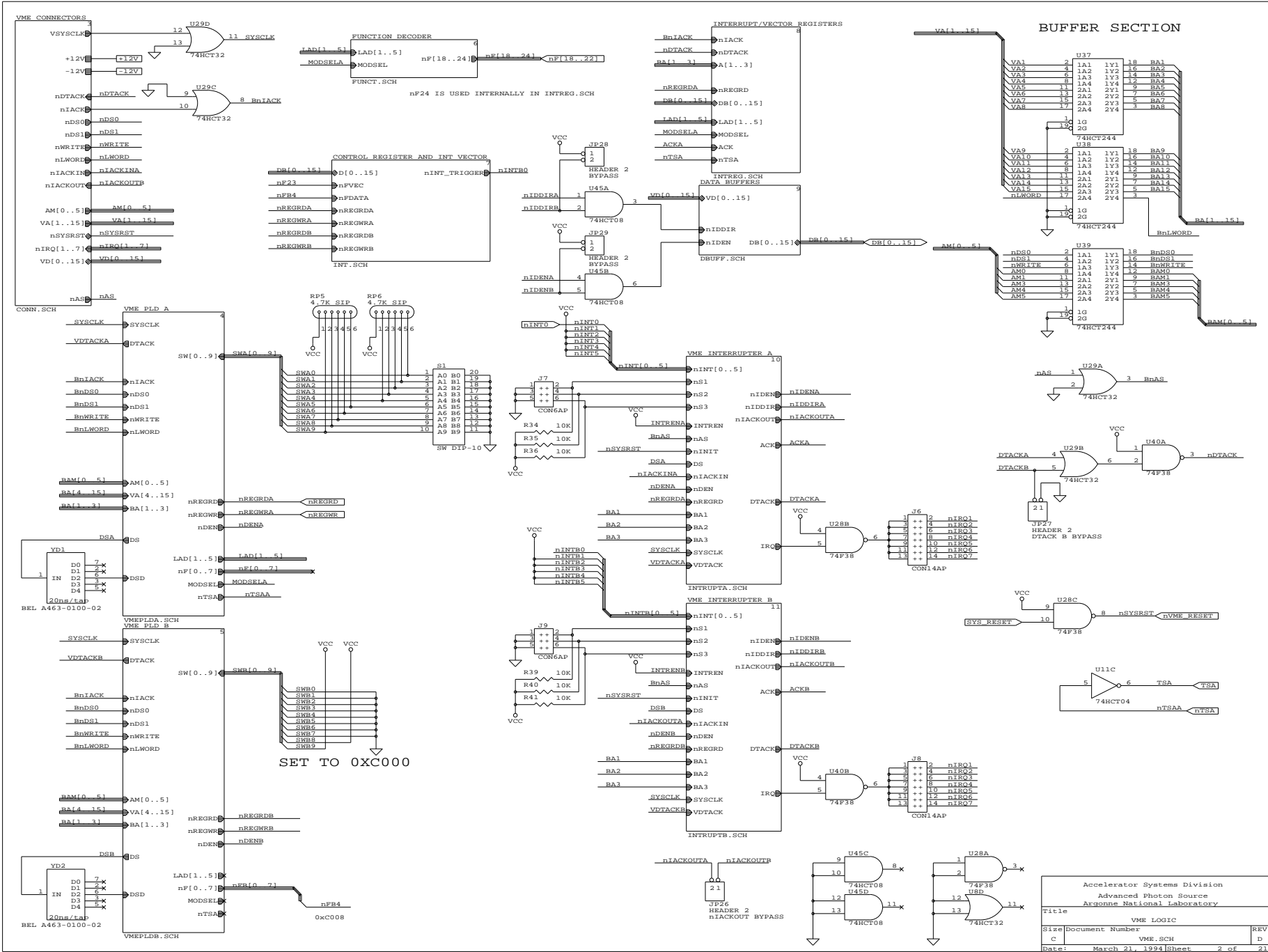
Parameter Name	Variable Type	Corresponding Register
Di	BI - Reads the status	Digital inputs
Temperature	AI - Returns the temperature value	Temperature Monitor (in C)
BootWatchdog	BO - Turns on the automatic reboot	Enables Watchdog Reset
	BI - Reads the status	
Do	BO - Turns on the specified output	Digital outputs
	BI - Reads the status	
Led	BO - Turns on the specified LED	Status LEDs
	BI - Reads the status	
RxWatchdog	BI - Reads the status	Rx Watchdog has failed
RxTemp	BI - Reads the status	Rx Temperature is above setpoint
RxStat	BI - Reads the status	Rx CPU STATUS LED is off
RxRun	BI - Reads the status	Rx CPU RUN LED is off
Rx12v	BI - Reads the status	Rx 12 volt setpoint (OK)
Rx5v	BI - Reads the status	Rx 5 volt setpoint (OK)
RxFail	BI - Reads the status	Rx CPU FAIL LED is off
TxWatchdog	BI - Reads the status	Watchdog has failed
TxTemp	BI - Reads the status	Temperature is above setpoint
TxStat	BI - Reads the status	CPU STATUS LED is off
TxRun	BI - Reads the status	CPU RUN LED is off
Tx12v	BI - Reads the status	12 volt setpoint (OK)
Tx5v	BI - Reads the status	5 volt setpoint (OK)
TxFail	BI - Reads the status	CPU FAIL LED is off

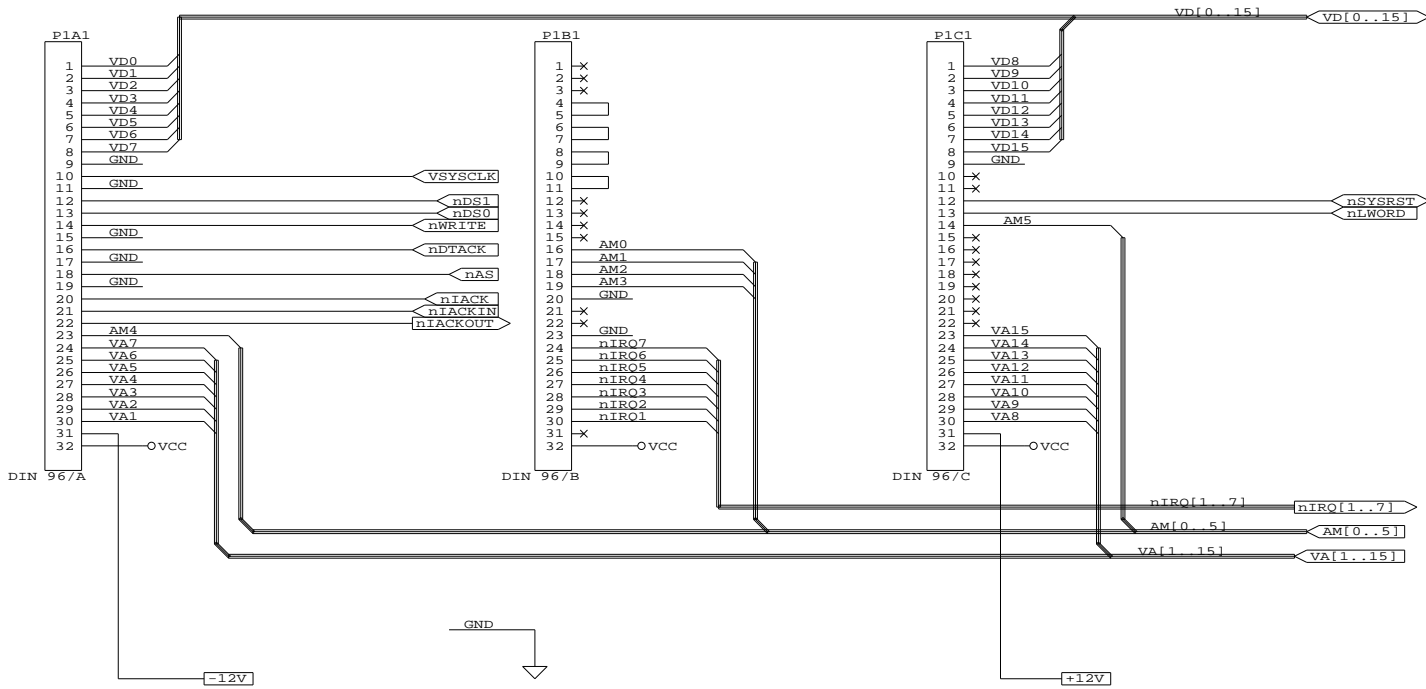


DAUGHTER BOARDS LOCATED IN:  
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 FOSER.SCH - FIBER OPTIC RS-232  
 ELECENET.SCH - 10 BASE-T  
 FOENET.SCH - 10 BASE-FO  
 STAT\_DB.SCH - FO STATUS LINK

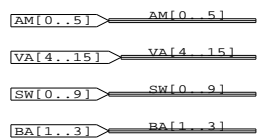
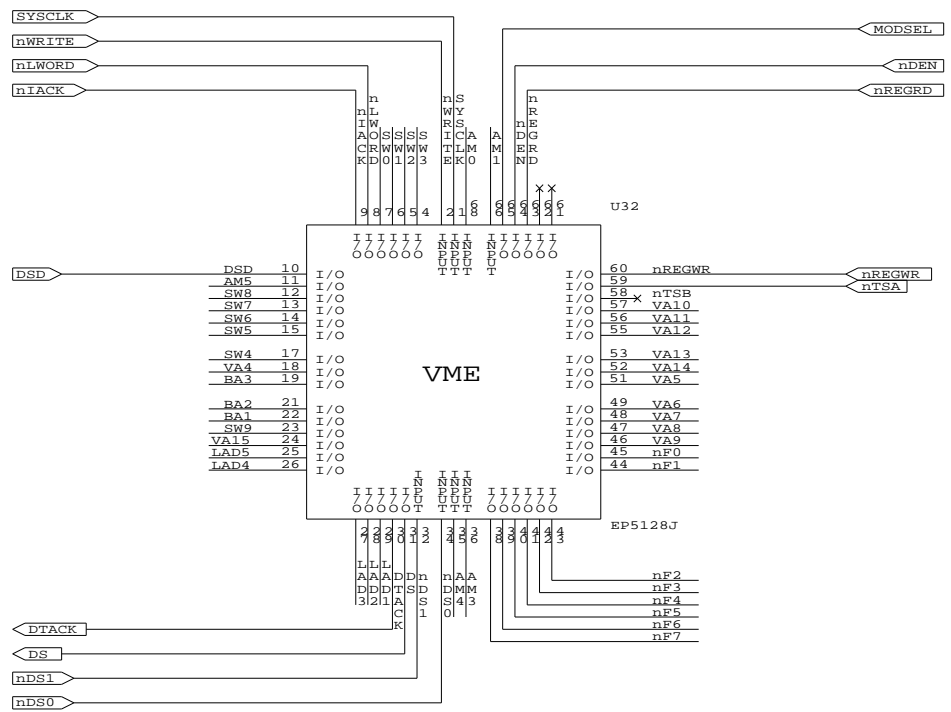
FIX INTERRUPTS  
 FASTER BINARY OUTPUTS  
 CLEAR\_BO ON RESET  
 GET RID OF VXI  
 FIX VOLTAGE MON

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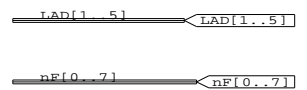




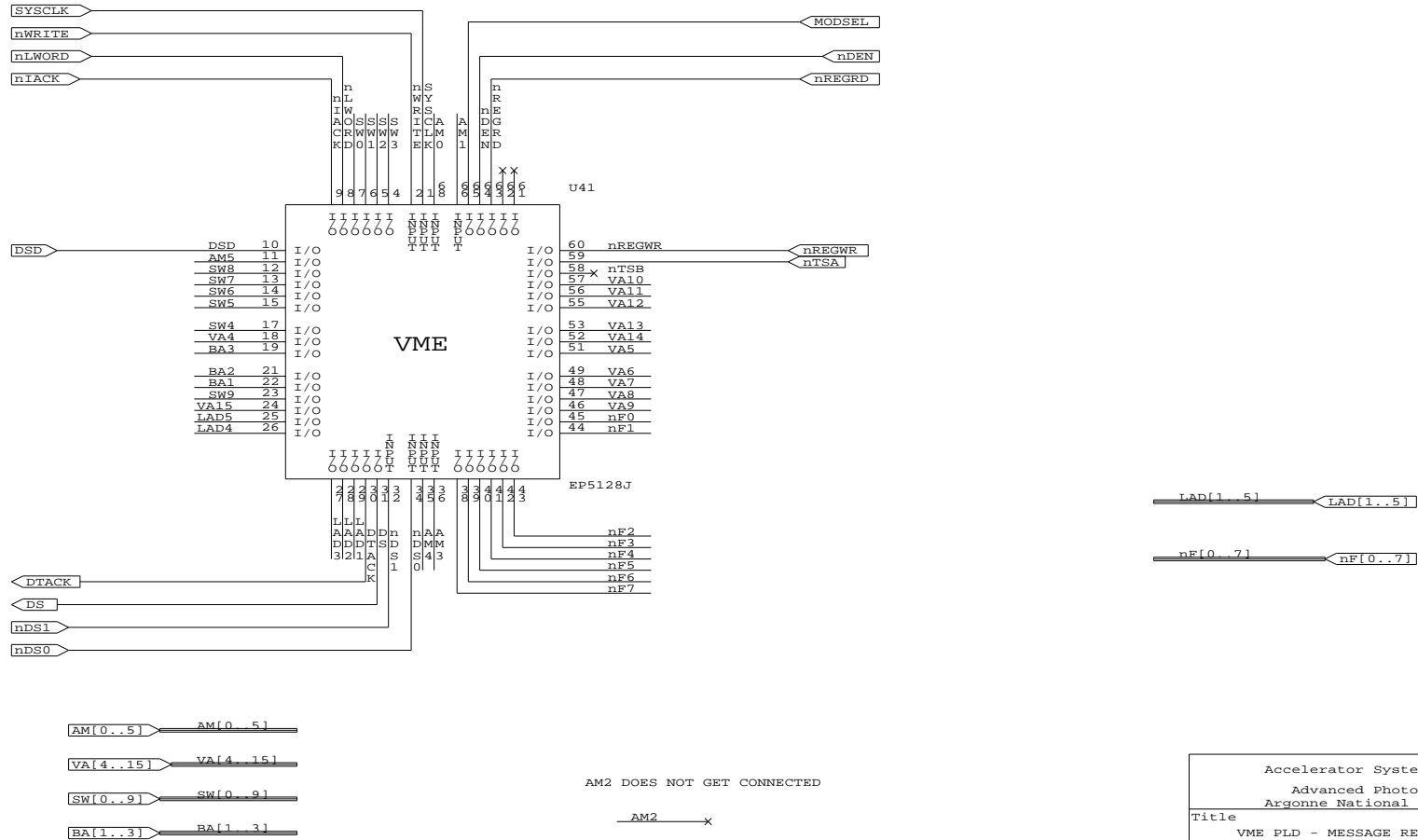
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Argonne National Laboratory		
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 → AM2 → x

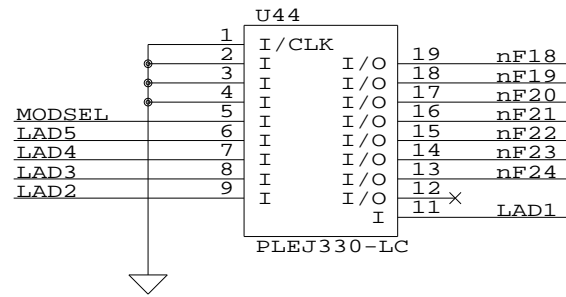
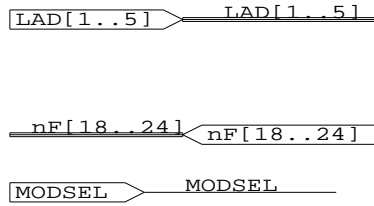


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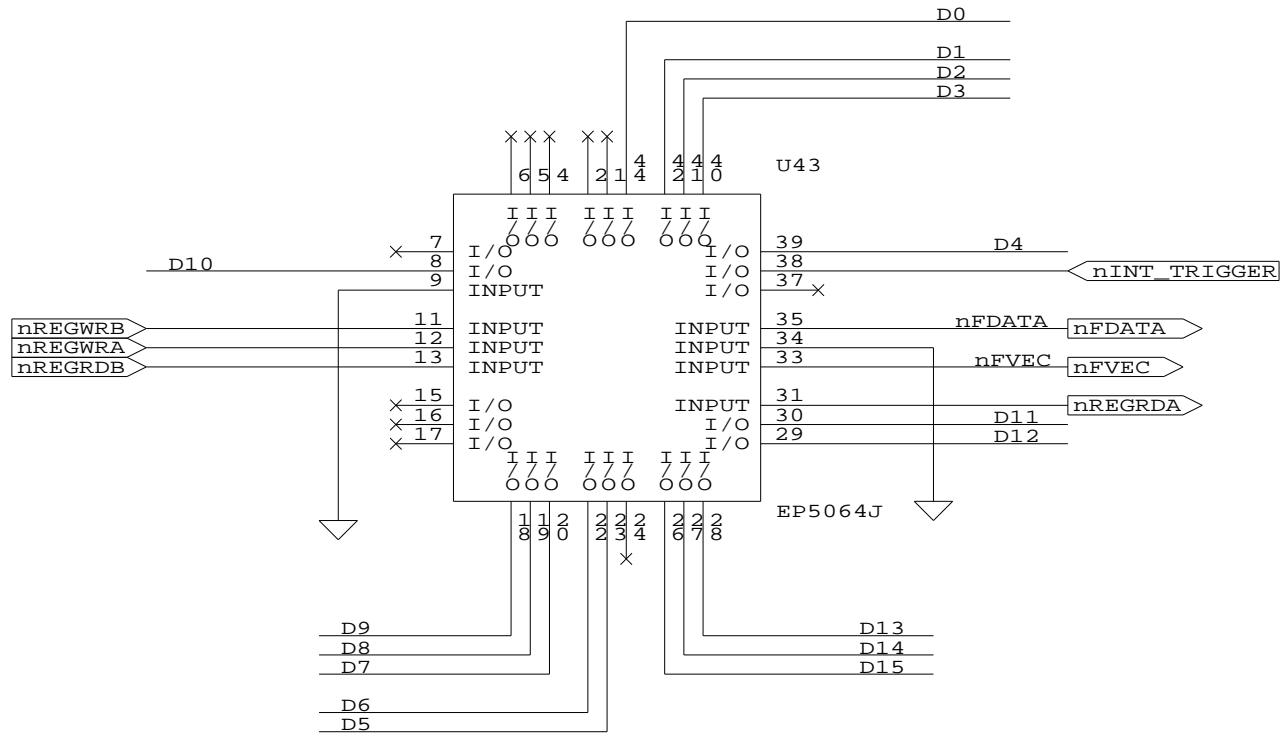




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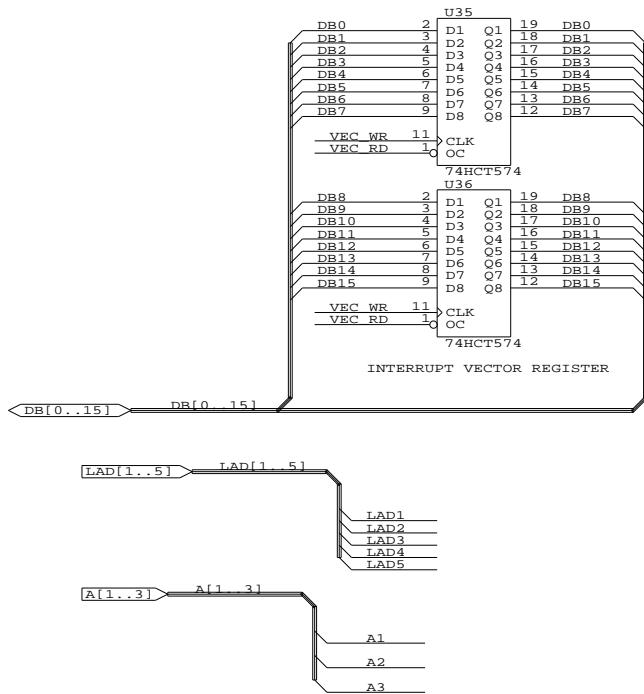
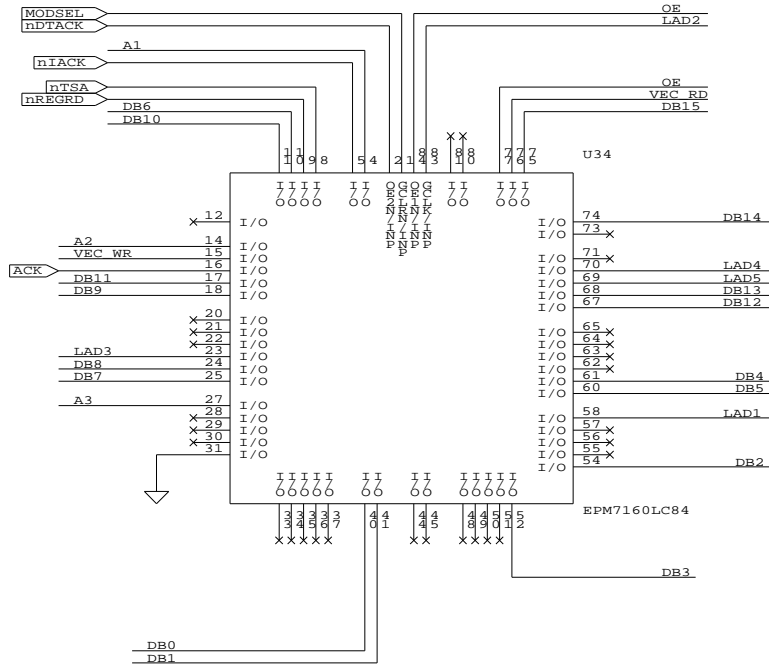
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Date:	March 10, 1994	Sheet 6 of 21



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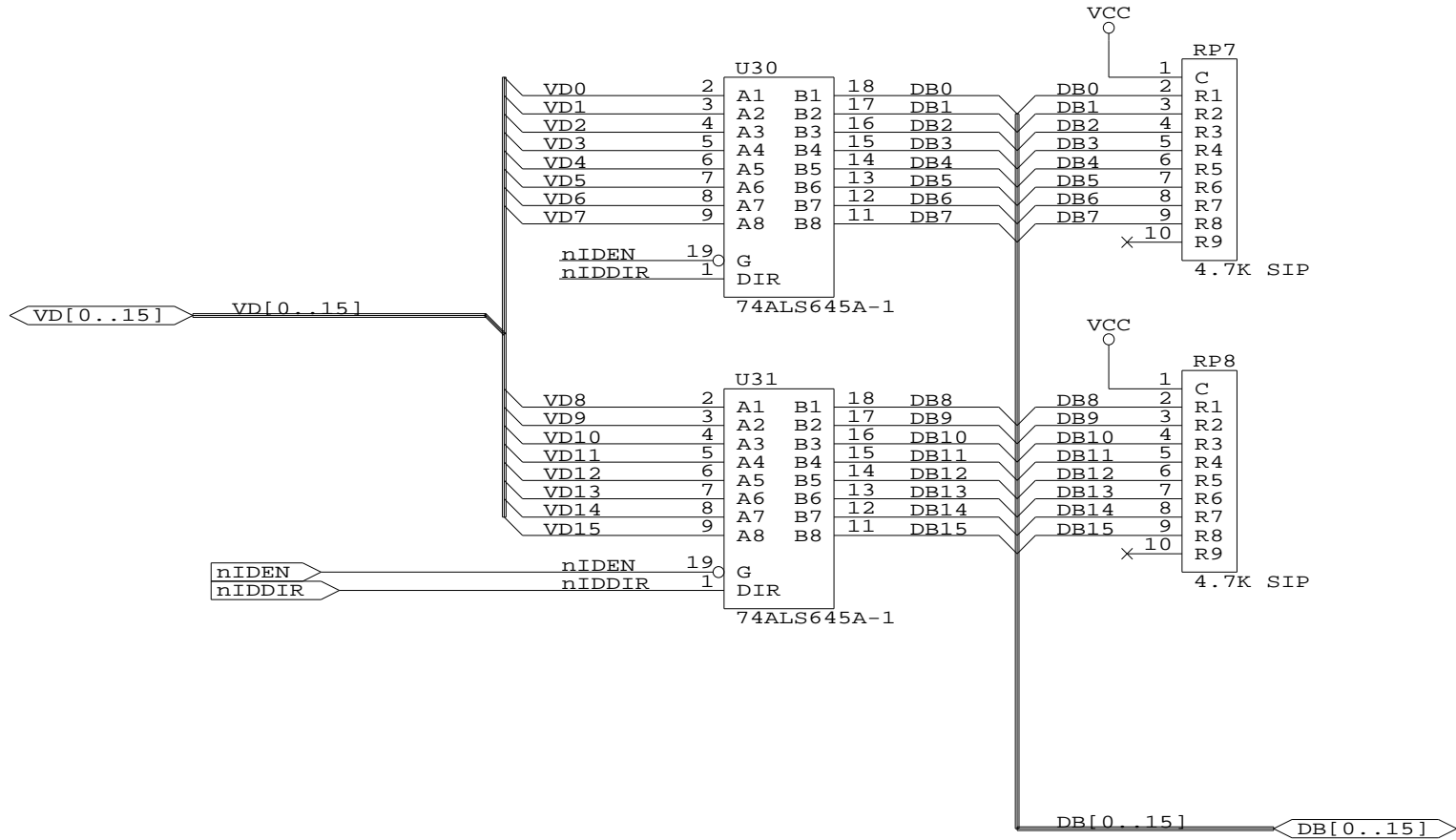
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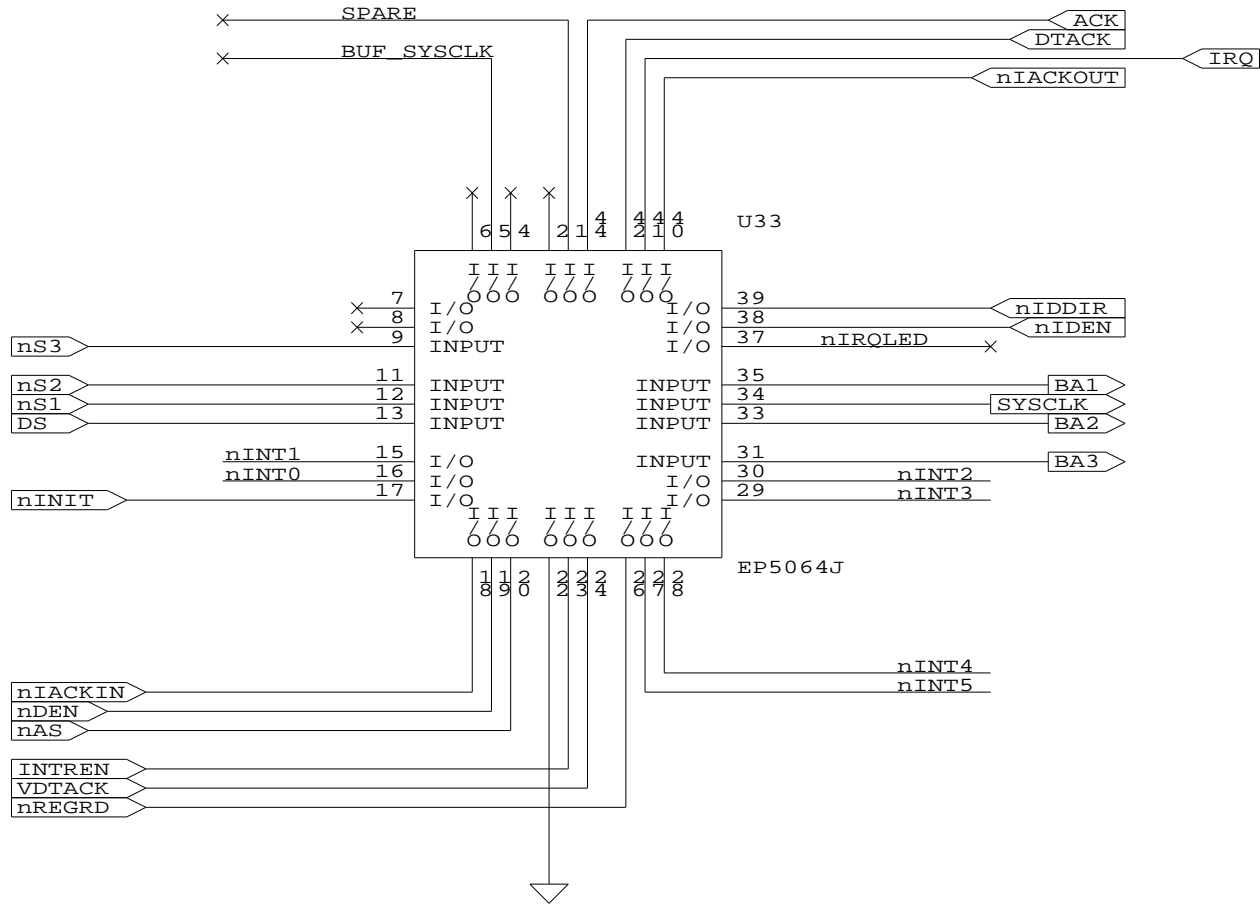


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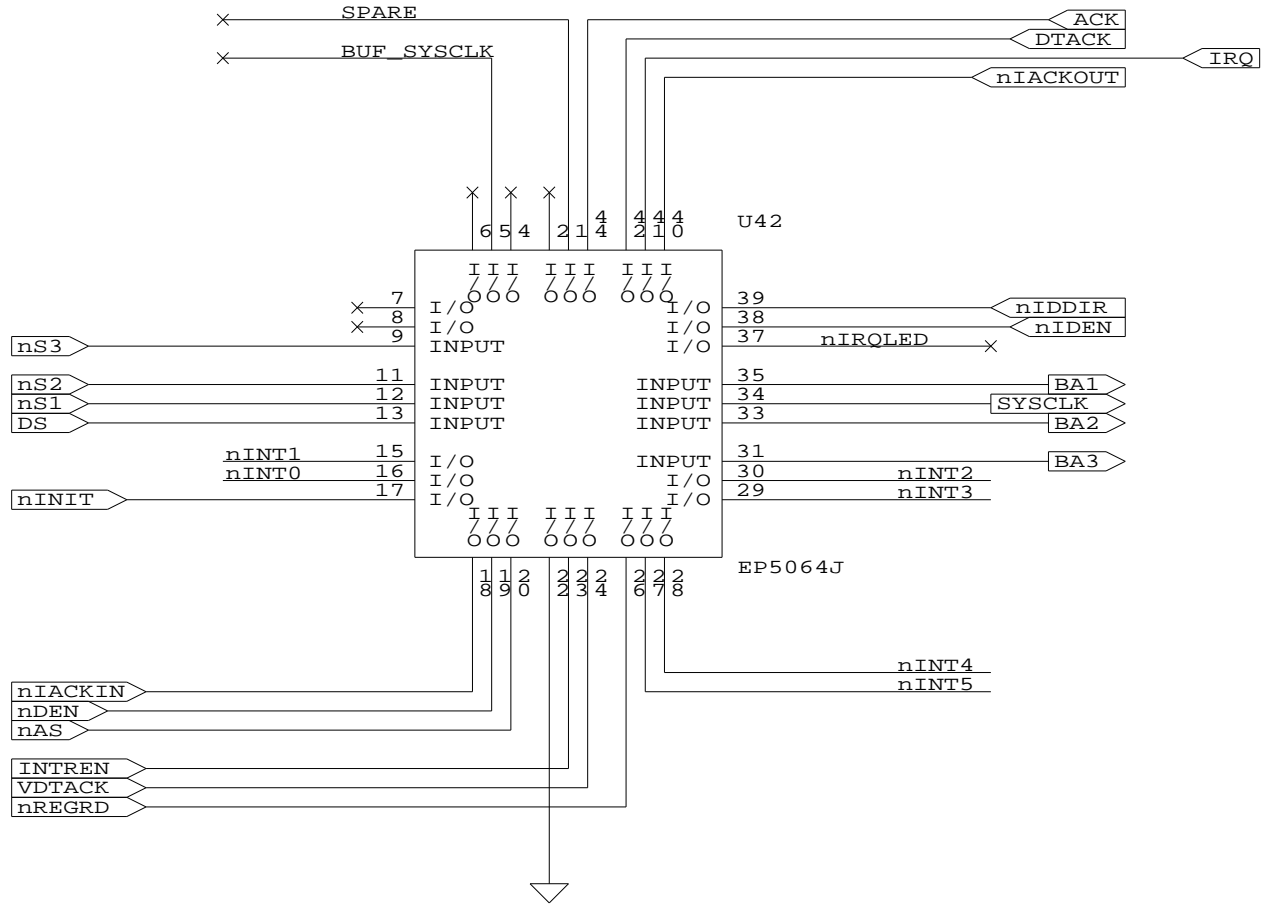


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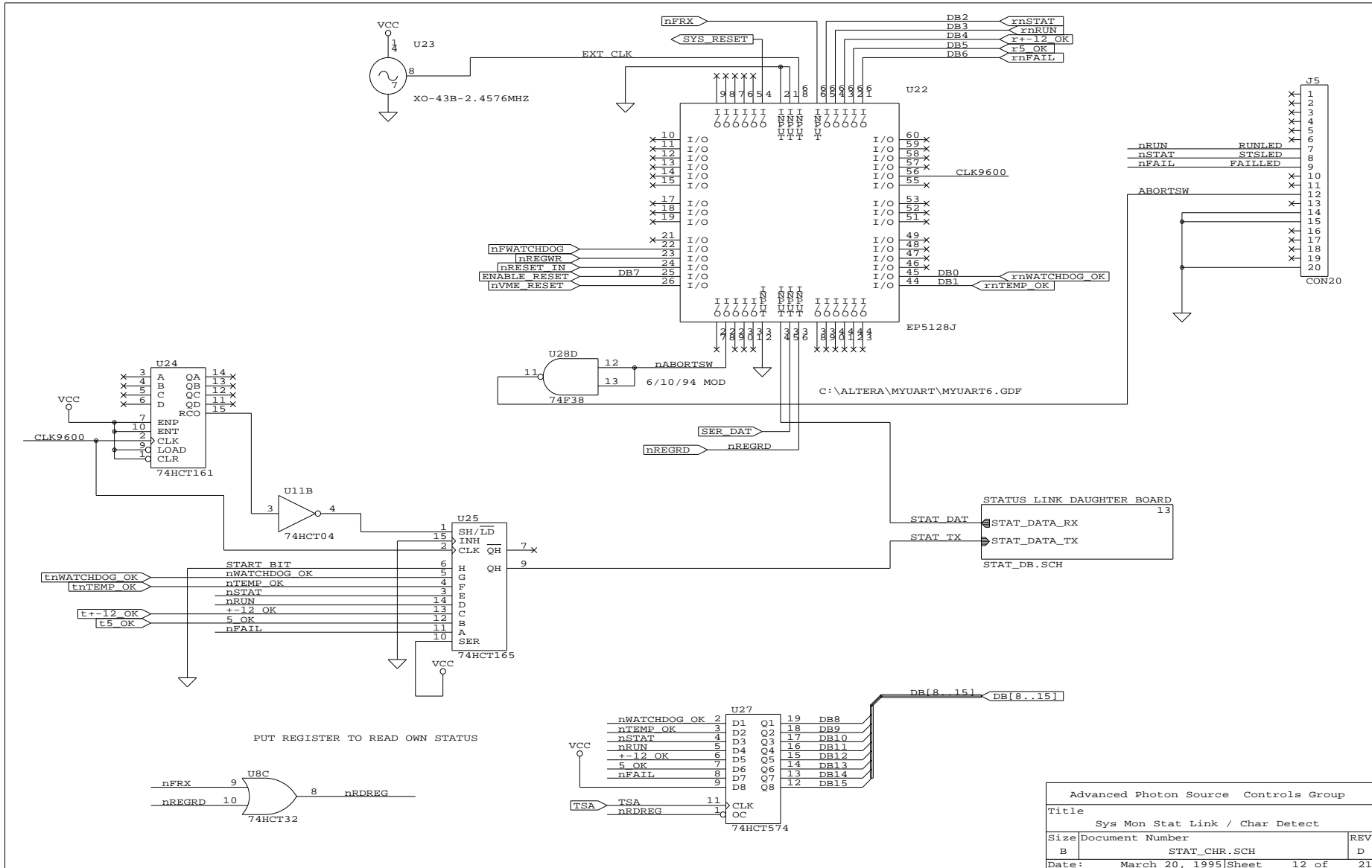
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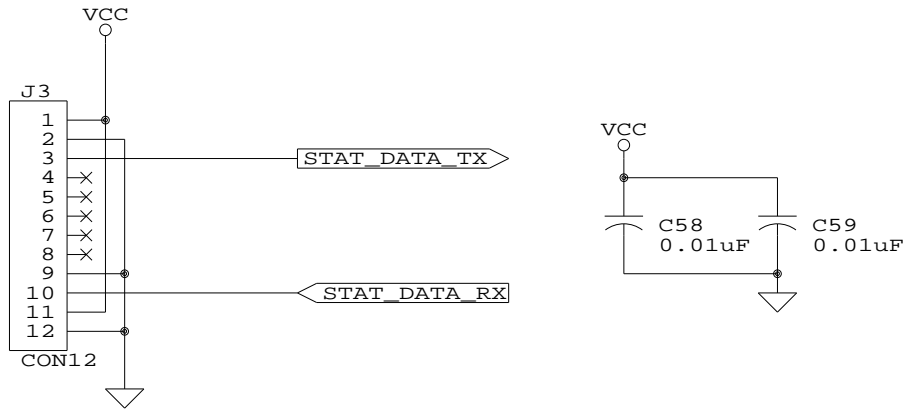
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nINT[0..5] → nINT[0..5]

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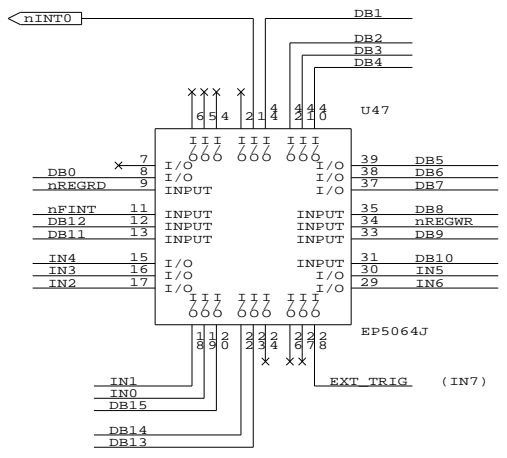
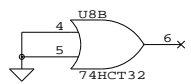
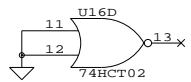
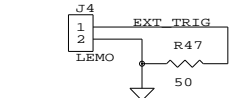
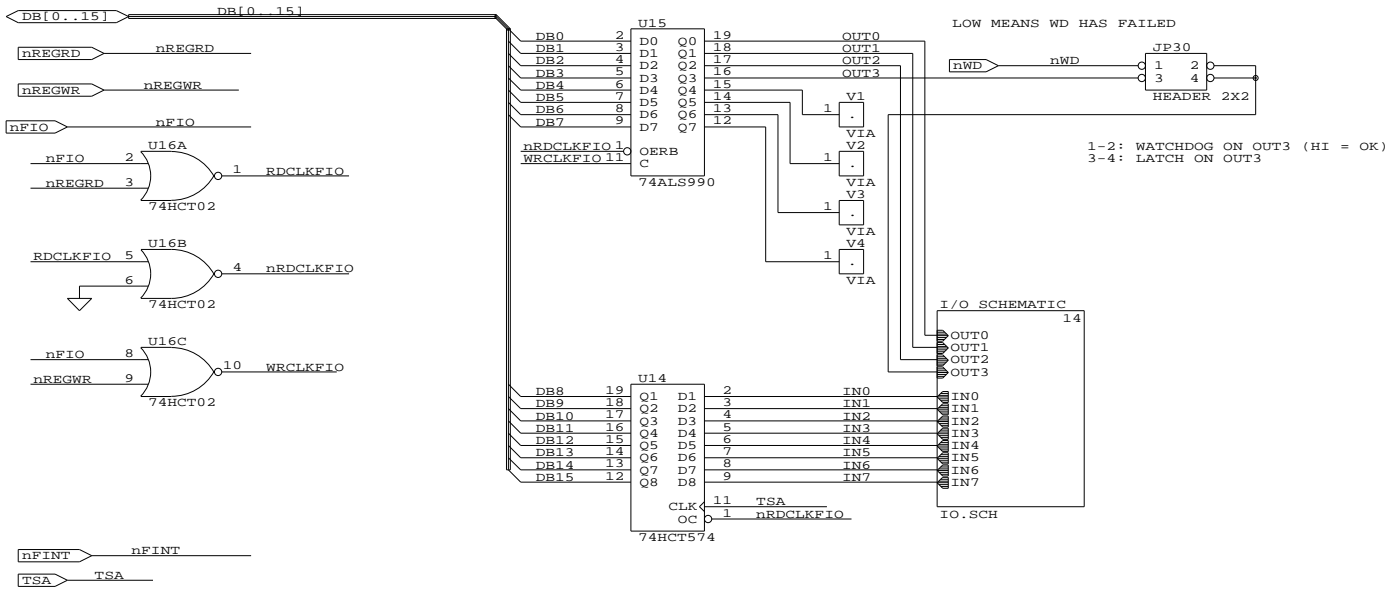




STATUS LINK  
 TRANSCEIVER DAUGHTER BOARDS  
 FIBER OPTIC OR ELECTRICAL

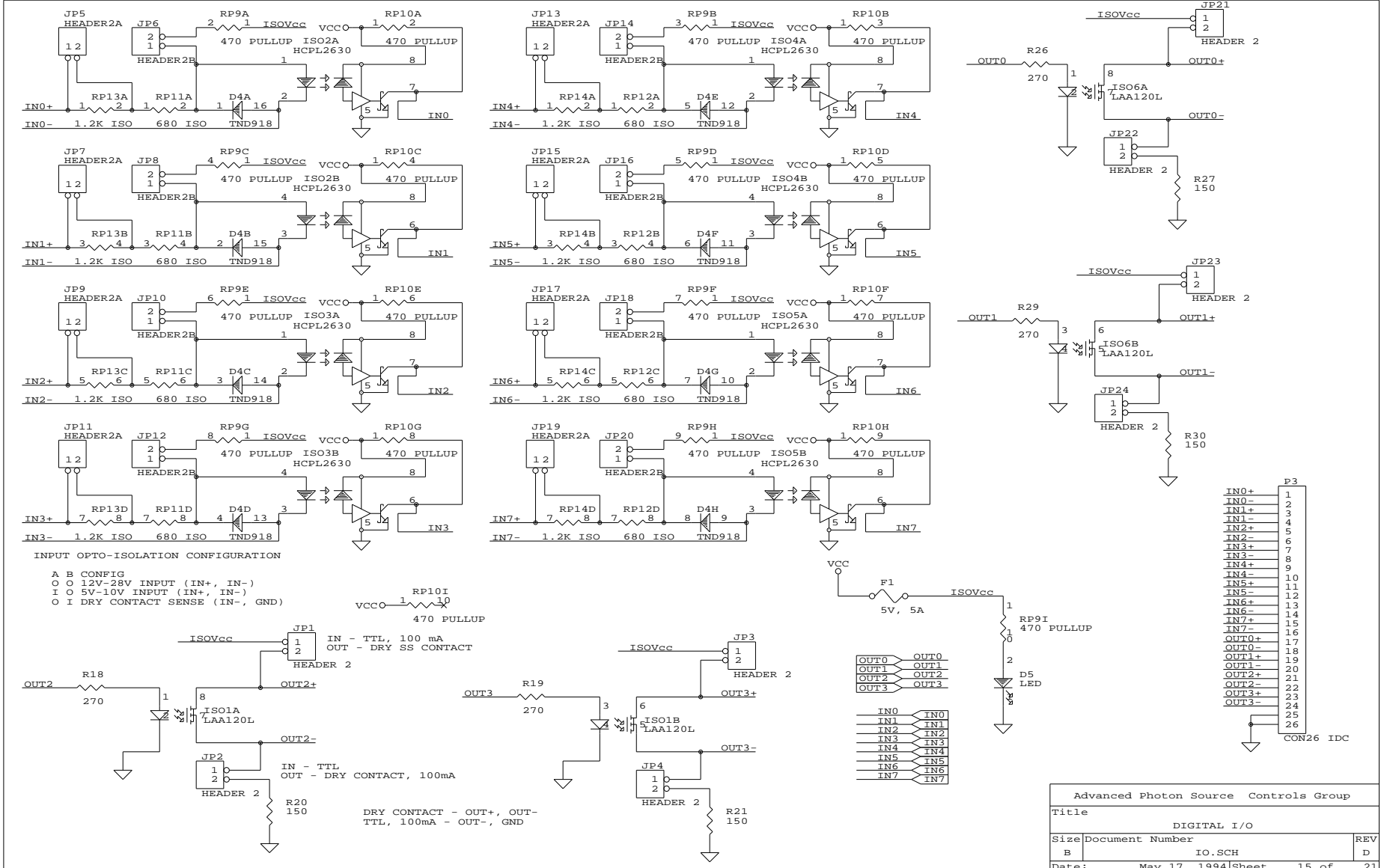
Advanced Photon Source - Controls Group		
Argonne National Laboratory		
9700 South Cass Avenue		
Argonne, IL 60517		
Title		
STATUS LINK DAUGHTER BOARD CONNECTOR		
Size	Document Number	REV
A	STAT_DB.SCH	C
Date:	March 10, 1994	Sheet 13 of 21



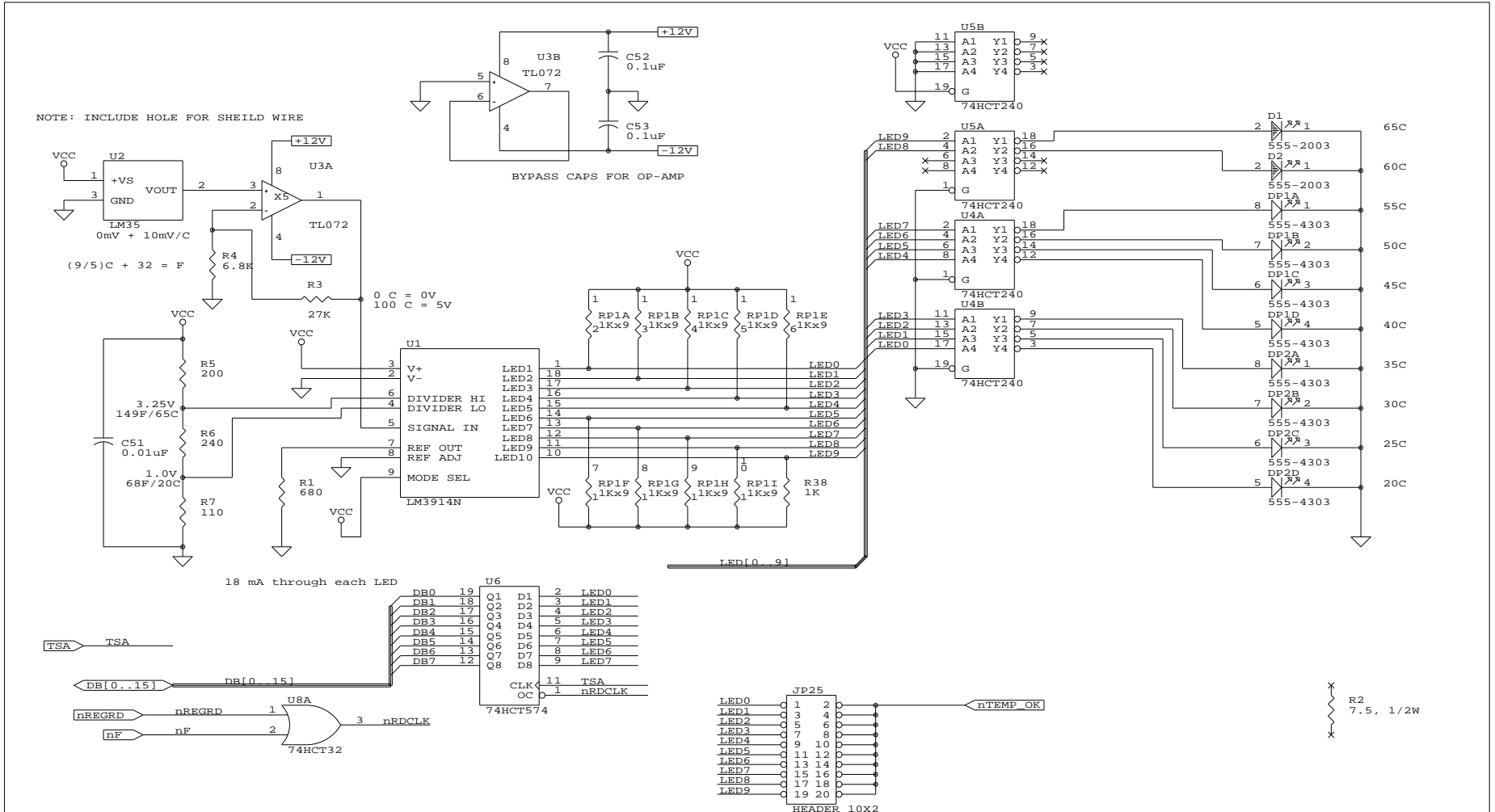


C:\ALTERA\SYSMON2\INTMASK.GDF

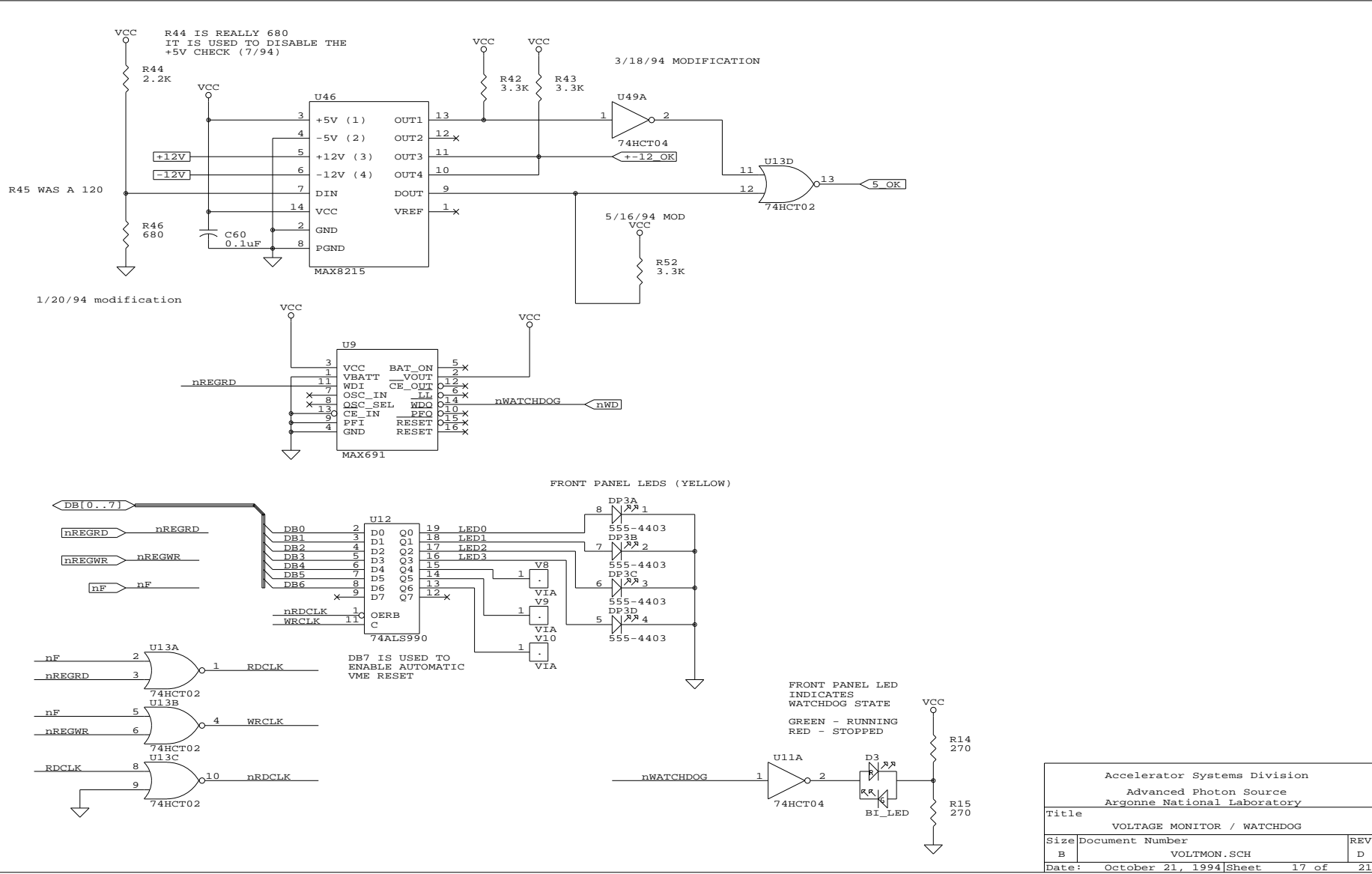
Advanced Photon Source Controls Group		
Title		
CONTROL FOR DIGITAL I/O		
Size	Document Number	REV
B	DIGIO.SCH	D
Date:	May 17, 1994	Sheet 14 of 21



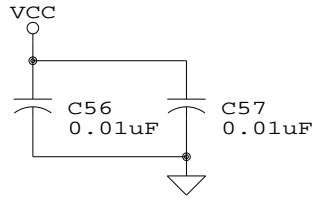
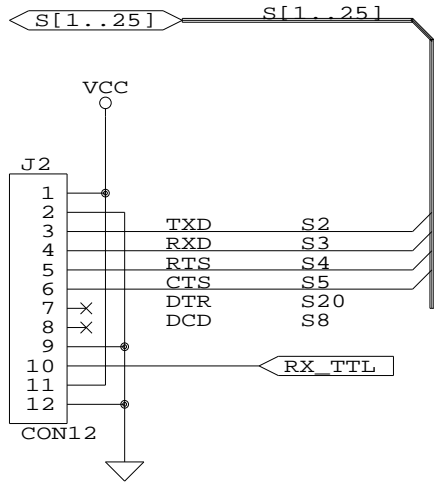
Advanced Photon Source Controls Group		
Title		
DIGITAL I/O		
Size	Document Number	REV
B	IO.SCH	D
Date:	May 17, 1994	Sheet 15 of 21



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Title		
TEMPERATURE MONITOR		
Size	Document Number	REV
B	TEMPMON.SCH	C
Date:	March 10, 1994	Sheet 16 of 21

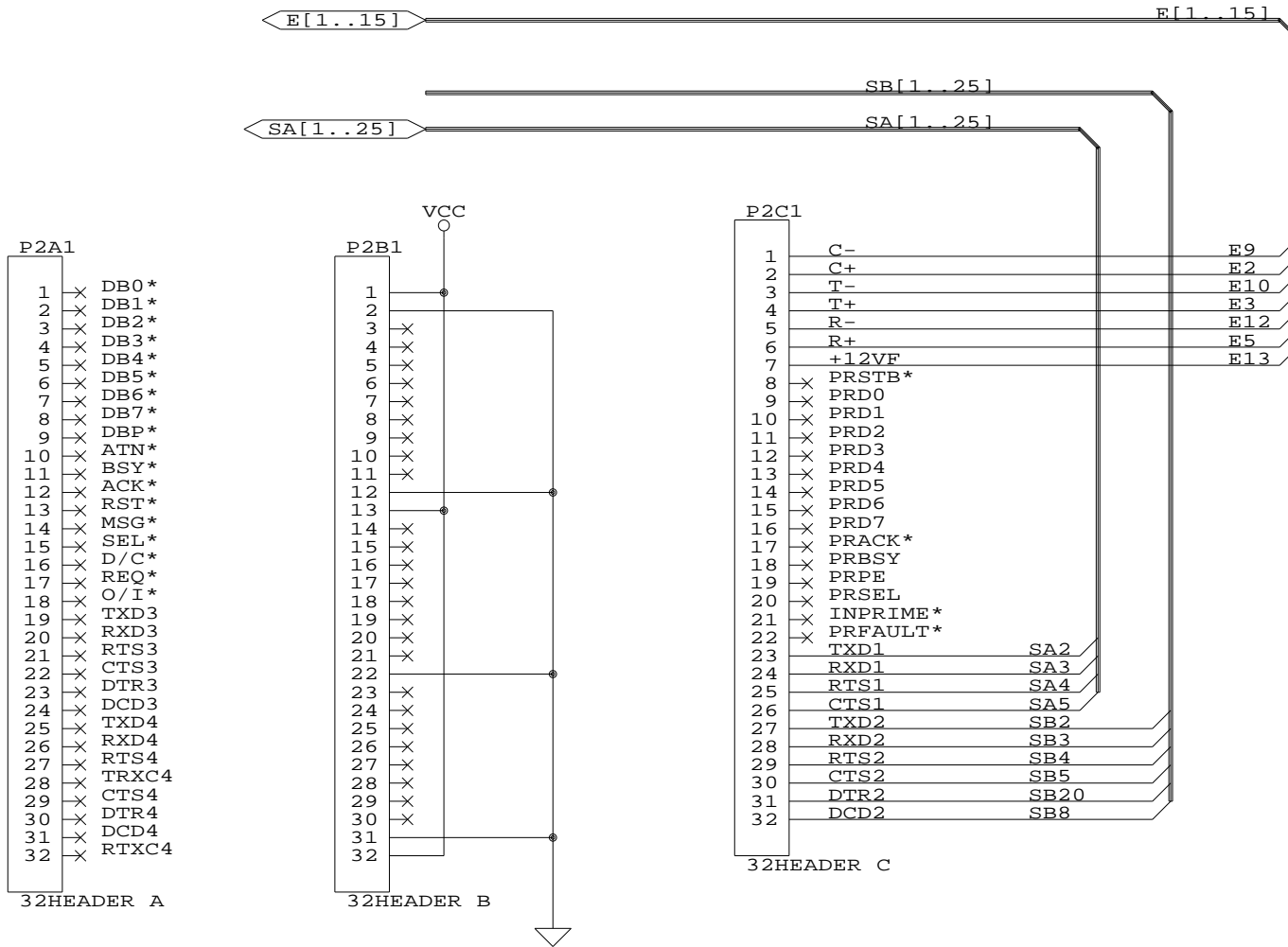


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Argonne National Laboratory		
Title		
VOLTAGE MONITOR / WATCHDOG		
Size	Document Number	REV
B	VOLTMON.SCH	D
Date:	October 21, 1994	Sheet 17 of 21

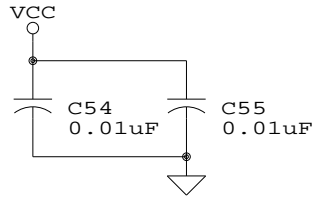
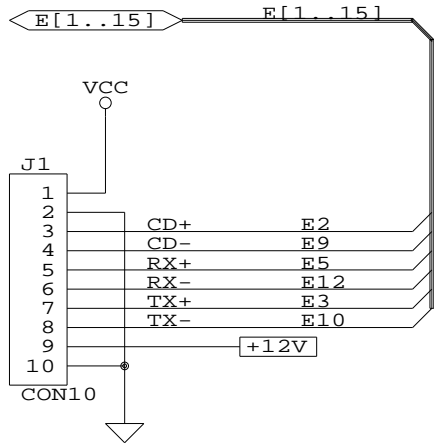


SERIAL PORT  
 TRANSCEIVER DAUGHTER BOARDS  
 FIBER OPTIC OR ELECTRICAL

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Advanced Photon Source Controls Group		
Title		
P2 CONNECTOR		
Size	Document Number	REV
A	P2.SCH	C
Date:	March 10, 1994	Sheet 19 of 21

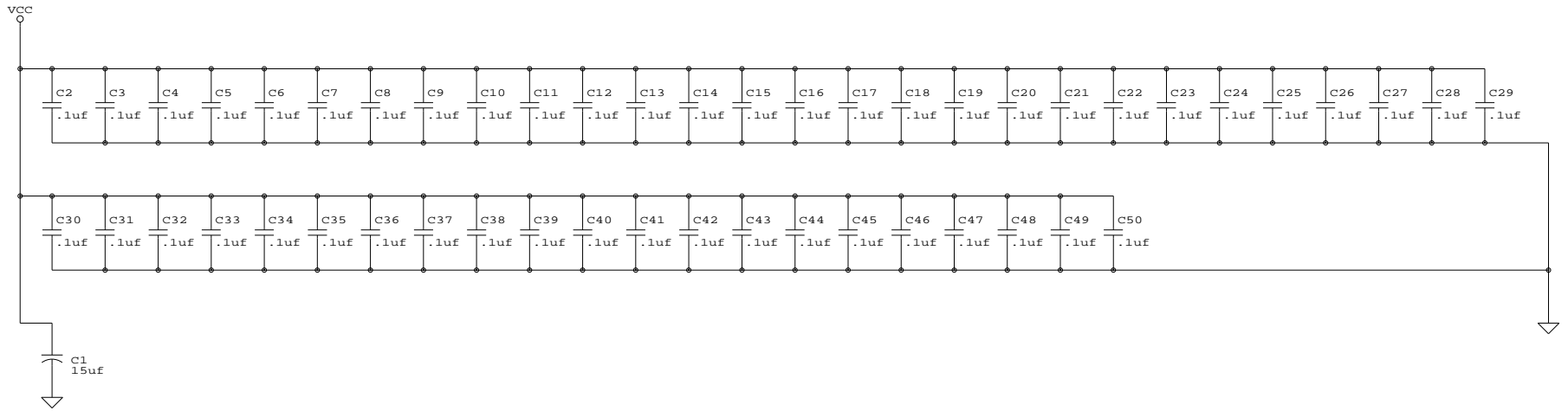


CONNECTOR FOR ETHERNET  
TRANSCEIVER DAUGHTER BOARDS

10 BASE-FO OR THINNET

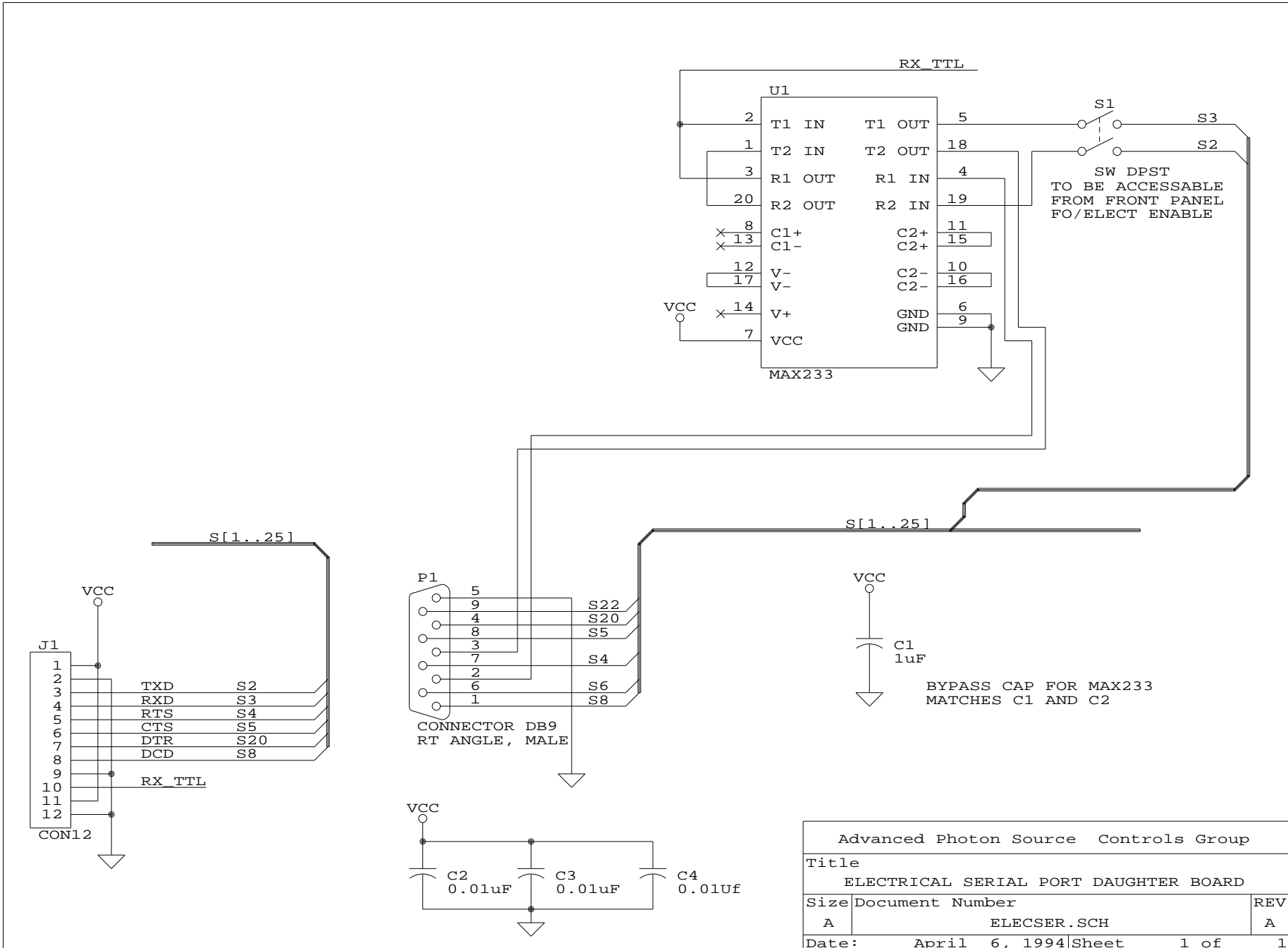
+12V - SOURCE UP TO 500mA  
COMMON - SINK UP TO 2A

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Title		
ETHERNET DAUGHTER BOARD CONNECTOR		
Size	Document Number	REV
A	ENETAUI.SCH	C
Date:	March 10, 1994	Sheet 20 of 21

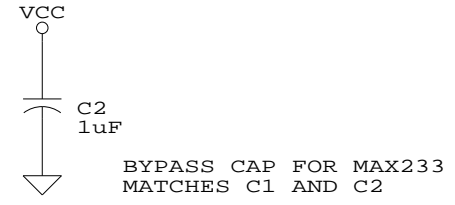
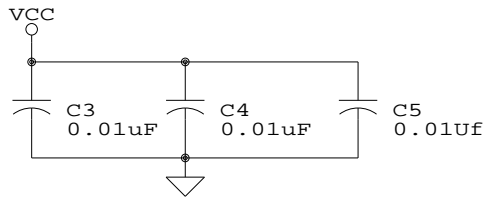
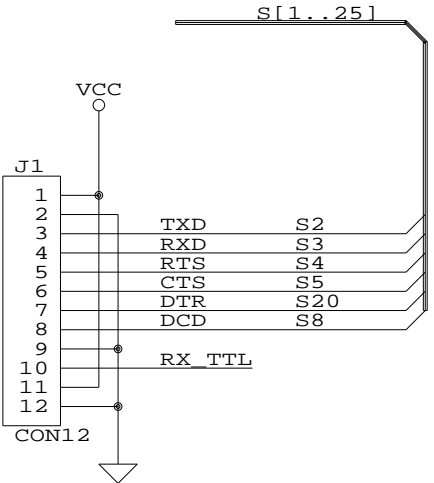
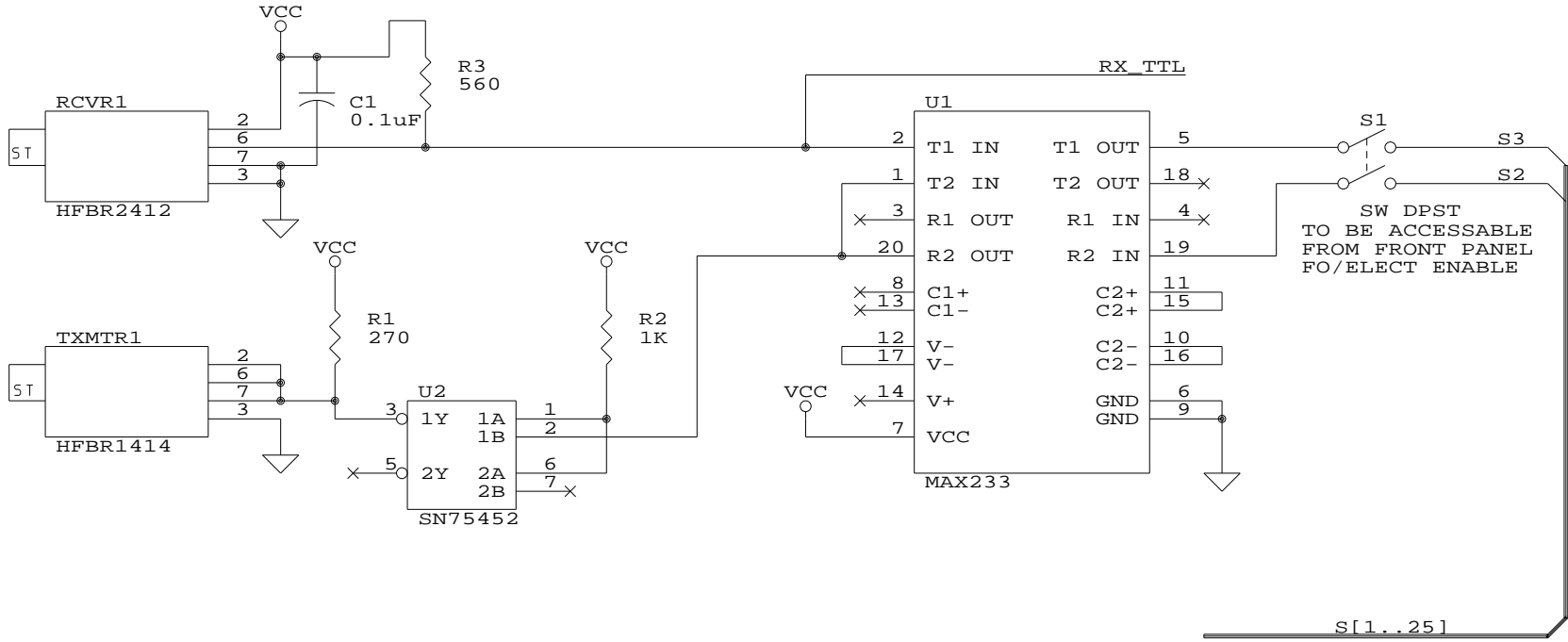


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Advanced Photon Source		
Argonne National Laboratory		
Title		
BYPASS CAPACITORS		
Size	Document Number	REV
B	BYPASS.SCH	C
Date:	March 10, 1994	Sheet 21 of 21

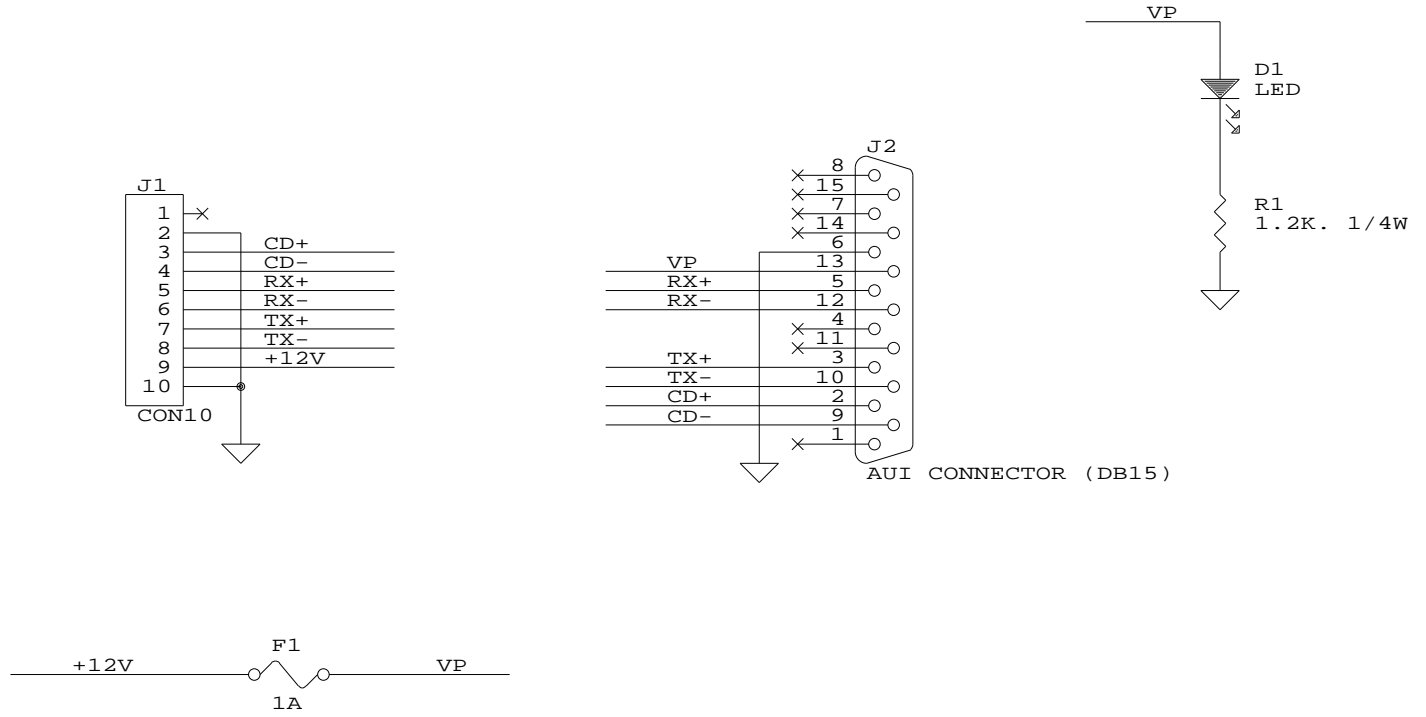




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Title ELECTRICAL SERIAL PORT DAUGHTER BOARD		
Size	Document Number	REV
A	ELECSER.SCH	A
Date:	April 6, 1994	Sheet 1 of 1



Advanced Photon Source Controls Group		
Title		
FIBER OPTIC SERIAL DAUGHTER BOARD		
Size	Document Number	REV
A	FOSER.SCH	
Date:	December 22, 1993	Sheet 1 of 1



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Title		
AUI CONNECTOR		
Size	Document Number	REV
A	AUIENET.SCH	
Date:	April 1, 1994	Sheet 1 of 1