64 CHANNEL, 32 BIT, READ ON THE FLY "VME" COUNTER / SCALER

MODEL VS64

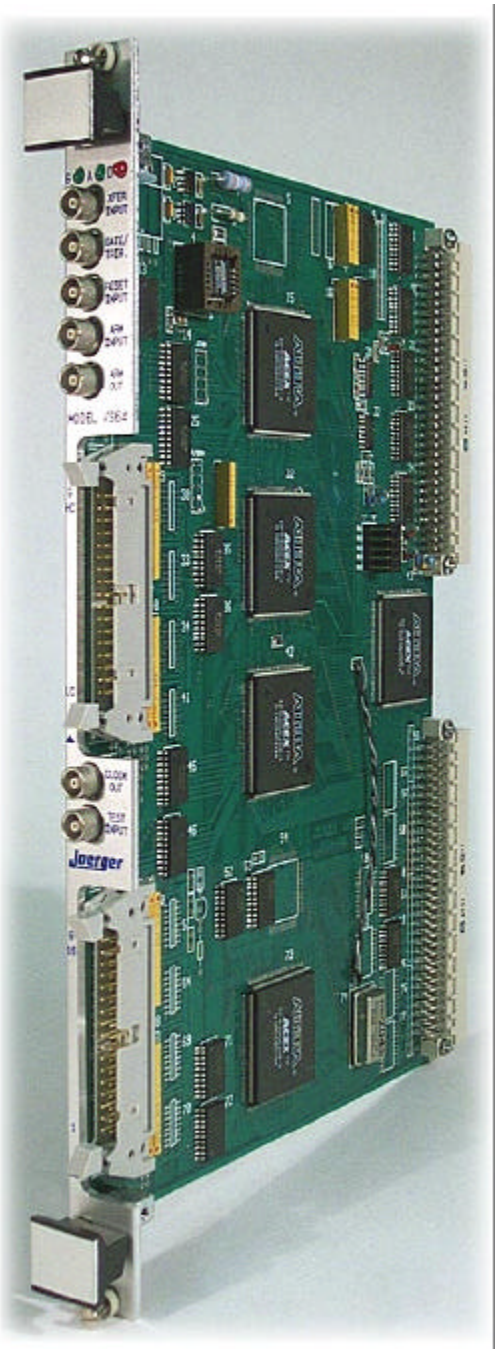
Joerger ENTERPRISES, INC.
166 LAUREL ROAD, EAST NORTHPORT, NY 11731 U.S.A.

MODEL VS64

- ***64 CHANNEL, 32 BIT, COUNTER / SCALER IN "VME" WITH " READ ON THE FLY " CAPABILITY***
- ***STAND ALONE PROGRAMMABLE PULSE OR GATE GENERATOR***

FEATURES:

- 64, 32 bit counter channels with 50 Mhz counting rate
- Stand alone programmable pulse or gate generator
- TTL, NIM, ECL input options for Count Inputs
- 16 Channel Version:
  - TTL, NIM, ECL with LEMO inputs or rear P2 access
- 32 Channel Version
  - TTL, NIM, ECL inputs with 34 pin ribbon connectors or rear P2 access
- 64 Channel Version
  - TTL inputs with 34 pin ribbon front panel connectors
- A16/A24/A32 D16/D32/BLT32
- A16 Base Address set with 5 jumpers, Control
- A24 Base Address software set, Module broadcast commands for multiple module control
- A32 Base Address software set, Extended address, Data
- Module Type and Serial Number Register
- Counter Transfer Registers for Readout
  Asynchronously Clock Transfer Registers from Front Panel or Software, no restrictions apply
  Counters and Overflows can also be cleared after the transfer, if enabled
- Read Channel N (previously registered data)
- Read and Clear Channel N (previously registered data)
- Read Channel N 'On the Fly' (clock only channel N register with new data)
- True 'READ ON THE FLY', no restrictions or gating needed
- Front panel gating compatible with VSC8/16; Gate In, Arm In, Arm Out
- Selective, Group and Global Count Enables
- Selective, Group and Global Counter Resets
- Selective and Group Overflow Enables for IRQ
- Overflow at 24 or 32 bits



- Three complete D08(O) Interrupters
  Interrupter#1 for 'OR' of selected Overflows
  Interrupter#2 for Front Panel Transfer Clock received
  Interrupter#3 for End of Gate
- Preset Programmable Gate, internal presettable counter which can be clocked with a selected clock signal or the active input from channel 1
- Front Panel Programmable Clock Output (default 10 MHz)
- Test Mode Selective by Group
  Front Panel Test Clock Input or Software Single Pulse
- Front Panel TTL Control Signals on LEMO connectors

The *JOERGER ENTERPRISES, INC.* Model VS64 is a 64 channel, 32 bit module that can operate in a counter or scaler mode and is packaged in a 6U, VME card. It is available with VME "Read on the Fly" capability at speeds in excess of 50Mhz. Counting is done with no prescaling or time outs so accuracy is ± 1 LSB. The counter or scaler mode is programmably selected. Gate times are crystal controlled and can be preset through the use of an internal presettable gate counter with either a programmable clock or the active signal on channel 1. The clock can be the internal crystal oscillator or an external input. The counter can be controlled by the front panel gate input or internally gated using the front panel trigger input or with a software command. TTL, NIM or differential ECL counter input signal levels are available. On ECL applications that require the input signals to drive latches or TDC's the input termination's are on sockets and may be removed. On the 16 channel module the counter inputs are Lemo. The 32 channel module uses a 34 pin ribbon connectors with two pins provided for each channel, one for the signal and one for the return. The 64 channel module accepts TTL inputs on two 34 pin connectors with a signal input for each channel and a common return. Rear access is available using connector P2 with either 16 or 32 channel TTL inputs. Transfer boards are available offering a variety of input connectors and signals, including fast RS422 using high speed, low voltage differential logic (LVDS). Analog inputs using comparators or V/F converters are available.

The Model VS64 can also operate as a stand alone, programmable output clock or gate generator. The clock can be selected from a count down generator using the 50Mhz crystal oscillator or the channel 1 input signal. The output is from the Clock Output connector, gate or clock are selected internally and can be triggered with the trigger input or programmably.

To provide versatile performance the module has 7 front panel control inputs. As with our Module VSC16 an Arm Input, Arm Output, a Gate/Trigger Input and a Clock Output are provided. This allows one or more modules to be armed and gated. The module's Arm Input is biased on and can be used to control one or more modules in a system with the Arm Output or an external signal. The clock output is programmable and crystal controlled. In addition, a Reset Input and Test Input are provided to make maximum use of the modules capabilities. A synchronous Data Latch signal is provided to latch the data in all channels. These are all TTL inputs via Lemo connectors.

To provide for a wide variety of applications the channels can be controlled individually, in banks of 16, globally or in a broadcast mode for multiple module control using A24 commands. Each channel's data and overflow can be reset similarly. To test the module a test pulse can be triggered internally or the front panel test signal can be used. For more extensive testing an internal or external gate signal can be used and a signal source like our clock output signal connected to the test input. The module may be read out in 3 modes, read, read and reset or "read on the fly". Read: reads out the data loaded into each channels register the last time it was latched. It can also read in block transfer mode (BLT32). Read and reset: reads a channel and resets it. A channel can also be "read on the fly" by addressing a

channel in that mode. This latches its counter's data into its register at that time and reads it out. The counters have been designed so that its accuracy is ±1 lsb in all modes. No prescaling or time outs are required.

Three separate interrupts are provided. One when the module receives a latch signal from the front panel, the second when an enabled channel has overflowed and the third when a gate signal ends. An 8 bit word can be stored for readout for each interrupt.

SPECIFICATIONS:

COUNTER INPUTS

TTL	Negative going TTL, 1k Ω to +5V Positive going TTL with 50Ω to ground is optional
NIM	- 600mv, 50 Ω to ground
ECL	ECL levels, termination's on sockets for removal if required

CONTROL INPUTS

GATE / TRIGGER INPUT	Gate: Active high TTL, 1k Ω to +5V (enabled) Trigger: Negative going TTL
ARM INPUT	Active high TTL, 1k Ω to +5V (enabled)
LATCH DATA INPUT, (XFER)	Negative going TTL, 1k Ω to +5V, clocks all counter transfer registers
TEST INPUT	Negative going TTL, 1k Ω to +5V
RESET INPUT	Active low TTL, 1k Ω to +5V

CONTROL OUTPUTS

ARM OUTPUT	Active high TTL output
CLOCK/GATE OUTPUT	TTL, Programmable, 10Mhz at power up, oscillator stability .01%

OPERATION

OPERATING SPEED	50Mhz minimum
ACCURACY	± 1LSB
CAPACITY	32 Bits

SIZE	SINGLE WIDTH, 6U VME CARD
POWER	+5V, (-12V WITH ECL OR NIM INPUT OPTIONS)

STANDARD MODULE: 32 CHANNELS, TTL INPUTS, SIGNAL AND RETURN PIN PER CHANNEL, TWO 34 PIN INPUT CONNECTORS

OPTIONS:

1) 16 CHANNELS LEMO INPUTS
2) 64 CHANNELS, TTL INPUTS, SINGLE PIN PER INPUT, COMMON RETURN
3) ECL SIGNAL INPUTS, 16 OR 32 CHANNELS
4) NIM SIGNAL INPUTS, 16 OR 32 CHANNELS
5) POSITIVE GOING TTL SIGNAL INPUTS
6) REAR ACCESS, TTL INPUTS, 16 OR 32 CHANNELS

JEI1102

Joerger ENTERPRISES, INC.
166 LAUREL ROAD • EAST NORTHPORT, NY 11731, USA
1-631-757-6200 • FAX 1-631-757-6201 • Email: info@joergerinc.com • web: www.joergerinc.com

Table of Contents

MODEL VS64, VME MULTICHANNEL COUNTER/SCALER & STAND ALONE CLOCK/GATE GENERATOR

The VSC64 is a 6U VME Slave and multiple Interrupter module that contains sixty-four, 32 bit scaler (counter) channels, 2 programmable clocks, an internal gate generator, and a separate Clock/Gate Generator along with the VME bus interface. The board appears to the bus as a 2k byte block of addresses in short or extended address space.

FEATURES

- 64 Channels, 50 MHz counting rate, 32 bit depth each channel
- Stand alone Clock/Gate Generator with front panel output
- Broadcast Command Addressing, groups of modules may be simultaneously addressed (programmable)
- TTL, NIM, ECL input options for Count Inputs
  - 16 Channel Version:
    - TTL, NIM, ECL inputs, rear P2 access, or front panel LEMO
  - 32 Channel Version
    - TTL, NIM, ECL inputs, rear P2 access, or 34 pin ribbon connectors
  - 64 Channel Version
    - TTL inputs with 34 pin ribbon front panel connectors
- A16/A24/A32 D16/D32/BLT32
- A16 Base Address set with 5 jumpers
- A24 and A32 Base Addresses software set (A24 for Broadcast Commands only)
- Module Type and Serial Number Register
- Counter Transfer Registers for Readout
  Asynchronously Clock Transfer Registers from Front Panel or Software, no restrictions apply
  Counters and Overflows can also be cleared after the transfer, if enabled
- Read Channel N (previously registered data)
- Read and Clear Channel N (previously registered data)
- Read Channel N 'On the Fly' (clock only channel N register with new data)
- True 'READ ON THE FLY', no restrictions or gating needed
- Front panel gating compatible with VSC8/16
  - Gate In, Arm In, Arm Out
- Selective, Group and Global Count Enables
- Selective, Group and Global Counter Resets
- Selective and Group Overflow Enables for IRQ
- Overflow at 24 or 32 bits
- Three complete D08(O) Interrupters
  - Interrupter#1 for 'OR' of selected Overflows
  - Interrupter#2 for Front Panel Transfer Clock received
  - Interrupter#3 for End of Gate
- Internal Programmable Gate with Front Panel or Software Trigger
  (can be a stand alone 'Gate/Pulse Generator')
- Front Panel Programmable Clock/Gate Output (Channel 1 input can be selected as source)
- Programmable Reference Clock for channel 1
- Test Mode Selective by Group
  - Front Panel Test Clock Input or Software Single Pulse
- Front Panel TTL Control Signals on LEMO connectors

VME Addressing

The following AM Codes are used:

AM 2D or 29	Short Address A16	D16/D32
AM 09 or 0D	Extended Address A32	D16/D32
AM 0B or 0F	Extended Block Transfer BLT32	D32 only

The board occupies 2 Kbytes of address space in VME addressing modes A16 or A32. The A16 Base Address is set with 5 jumpers selecting A11 - A15. The A32 Base Address is software settable in 2 registers at A16 Base+ 404h & 406h. These 2 registers set A11 to A31 and can only be accessed in A16 mode to prevent accidental overwriting the A32 address while in an A32 cycle. All other standard access use either A16 or A32 addressing.

BROADCAST COMMAND ADDRESSING (A24)

The same command can be issued to multiple VS64 modules by enabling A24 Broadcast mode. The A24 address and setup are stored at address 0x416. VS64 modules with the same A24 address will accept the commands to that address. One VS64 is setup as the master and all the others with the same A24 address are setup as slaves. Only write cycles are accepted. Many different groups of modules may be created using different A24 addresses. This is particularly useful to arm, trigger or disarm modules as a group.

Power-up, Sysreset and Master Reset

Set all registers and storage elements to default value. The default value is false (0 or reset) for all except the 4 Selective Count Enable Registers and the Group Selective count Enable Registers whose default is true (1 or set).

FRONT PANEL SIGNALS

The module is available with TTL level Count Input signals. All input and output control signals are TTL level and use single pin LEMO connectors: TTL inputs have 1Kohm pullup resistors to +5 volts.

Control Signals	
Clock Out	Continuous programmable clock in Front Panel Gate Mode Gated programmable clock or Internal Gate in Triggered Modes Negative going edge, (positive going is optional) Gate output is Positive True
Arm Out	High true, controlled by software (base+ 42A and 42C) can be connected to Arm In
Arm In **	Input must be High (high true) for count enable, see count enable drawing
Gate/Trig In **	Input must be High (high true) for count enable in Gate Mode Negative going edge starts Internal Gate in Trigger Modes see count enable drawing
Reset	Low true input resets all channel Counters and Overflows, not Transfer Registers
Xfer Clock	Negative going edge clocks all Counter Transfer Registers
Test In	Negative going edge Counter Clock for channel groups in Test Mode (positive going is optional)
Counter Inputs	
Input 1-64 TTL	Negative going edge (positive is optional) 1Kohm pullup to +5v
Input 1-32 NIM	Negative going edge 50ohm to ground
Input 1-32 ECL	Negative going edge

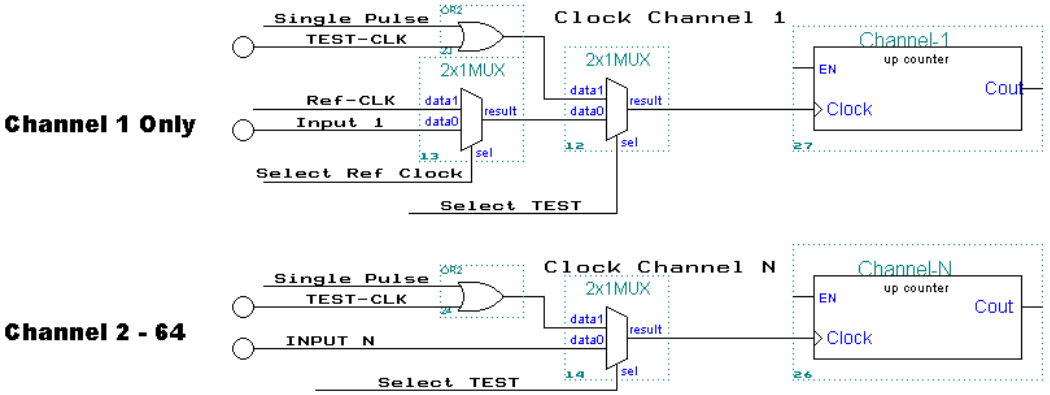
Note: ** input biased true

COUNTERS

The 64 counter channels are broken up into 4 Groups of 16 channels. Each channel has a 32 bit counter,32 bit Transfer Register, Overflow bit and clock selection mux. There is also per channel and group control for gating and resets. The counter contents are only readout through the Transfer Register. This allows a 'snapshot' of all of the channel counters to be registered at the same time. The Transfer Register is clocked from the front panel 'Transfer Clock' input or a software generated clock. There are bits in the Control Register to enable clearing of all counters after the transfer. A special circuit design allows the Transfer Register clocks to be asynchronous and there will be no error in the registered data even if the counters are actively counting (at any speed). Read on the fly from a single channel is also available in which case only the Transfer Register for the addressed channel is updated for the readout. There is no dead time in the counting and no pulses are missed. In other words, the Transfer Clock can occur at any time with no regard to gating and with no errors in the registered data.

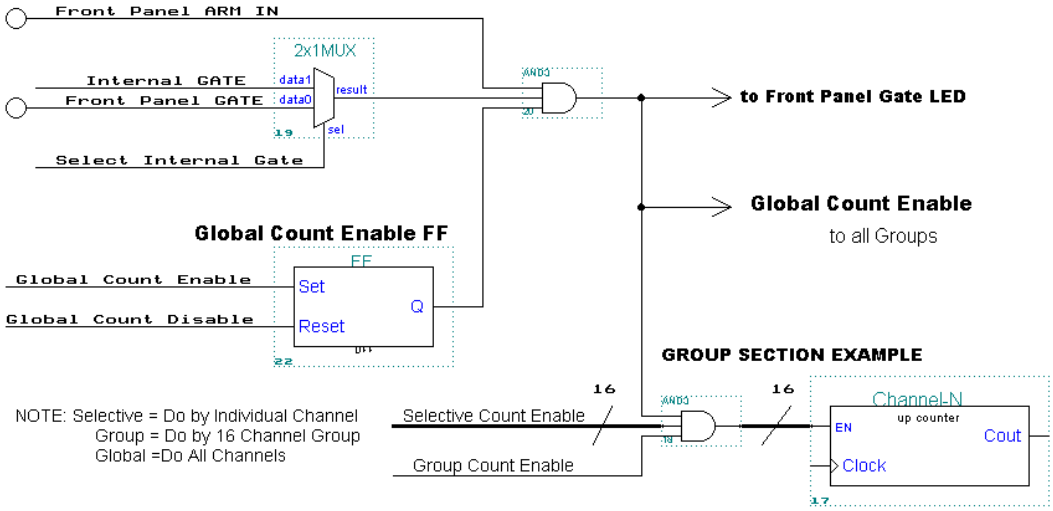
Each channel has an Overflow bit that can be set by the trailing edge of bit 24 or bit 32, can be enabled or disabled individually into the 'OR' for IRQ#1, and can be individually read out.

The clock for each counter is selected from the front panel input, test input or single pulse and in addition, for Channel 1 only, the Reference Clock.



Count Enable

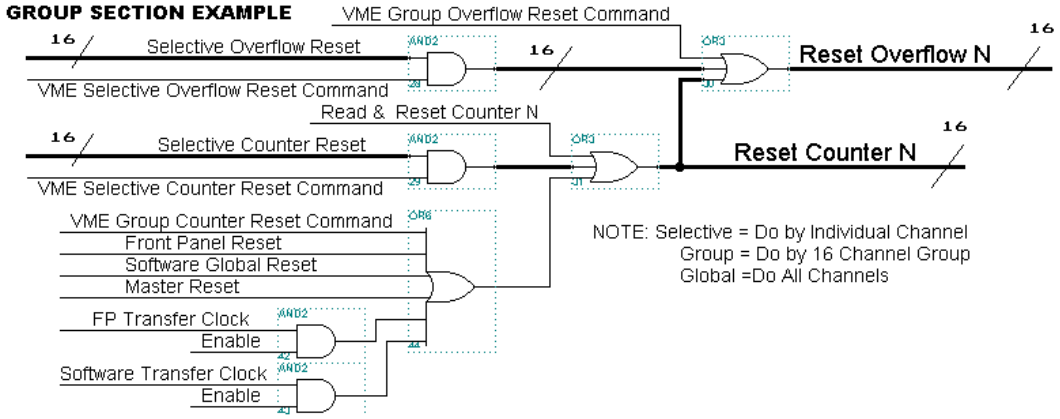
A channel counts the selected clock source if the following signals are all true: Front Panel Gate In, Front Panel Arm In, Global Enable, Group Enable and Selective Enable. All the previous signals default to true except the Global Enable which default to false (disabled). The Front Panel Arm In and Gate In are biased to true.



NOTE:	Selective = Do by Individual Channel
	Group = Do by 16 Channel Group
	Global =Do All Channels

Counter and Overflow Reset

The counter contents and associated overflow bits can be cleared Selectively or by Group via software, or Globally via software or the Front Panel Reset Input. Any valid counter clear also clears the associated overflow regardless of the setting in the Selective Overflow Reset Enable Register. See the diagram below.

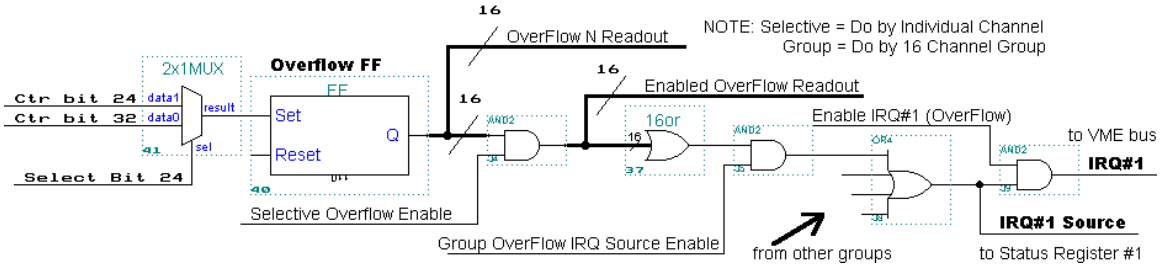


VME Interrupters

The module contains 3 complete D08(O) VME Interrupters. Interrupter#1 is the 'OR' of all enabled overflow bits. Interrupter#2 can be set on receipt of a front panel Transfer Register Clock. Interrupter#3 can be set at the end of the Gate, (labeled 'Global Count Enable' in count enable drawing above). There are registers to set the VME IRQ level, Status/ID word and enable/disable status for each interrupter. Each interrupter can be programmed to any IRQ Level (1 to 7, or none) including the same levels if desired. The IRQ sources may be used without using interrupts on the bus, see Status Register (base+ 400h).

Interrupter#1 - Overflow:

The counter overflow bit can be selected on a group basis for the trailing edge of either the 24bit or 32bit using base+31Eh. The overflow interrupt source is the 'OR" of any enabled channel overflow. The Selective Overflow Enable bit and Group Overflow Enable must be true. The VME IRQ Level and an enable/disable bit for this interrupt are programmed at base+ 40Eh and the Status/ID word is stored in base+ 408h. The source status can be read from Status Register. To clear IRQ#1 each participating channel overflow must be cleared or disabled since the IRQ source is the 'OR' of all enabled overflow bits



Interrupter#2 - Front Panel Transfer Clock Received:

This interrupt source will be set by the Front Panel Transfer Clock going true. The VME IRQ Level and an enable/disable bit for this interrupt are programmed at base+ 40Eh and the Status/ID word is stored in base+ 40Ah.. The source status can be read from Status Register. IRQ#2 is cleared and removed from the bus on IACK cycle acknowledge (ROAK), writing to base+ 432h with D0, disable IRQ#2 or Master Reset.

Interrupter#3 - Global Gate has Ended

This interrupt source will be set by the Global Count Enable Gate going false. The VME IRQ Level and an enable/disable bit for this interrupt are programmed at base+ 40Eh and the Status/ID word is stored in base+ 40Ch.. The source status can be read from Status Register. IRQ#3 is cleared and removed from the bus on IACK cycle acknowledge (ROAK), writing to base+ 432h with D1, disable IRQ#3 or Master Reset.

Readout

The counter data readout format is as follows:

D16 readout

Address	D15-D08	D07 - D00
A01 = 0	data bits 31 - 24	data bits 23 - 16
A01 = 1	data bits 15 - 8	data bits 7 - 0

D32 readout

D31-D24	D23-D16	D15-D08	D07 - D00
data bits 31 - 24	data bits 23 - 16	data bits 15 - 8	data bits 7 - 0

The counter/scaler data can be read from three different contiguous block of addresses. The actions carried out for a read to each block vary, but the data is always read from the Transfer Register and not directly from the counters.

Read Channel N:

For a single read (D16/D32) or block transfer (BLT32 only) to an address in this block (base+ 000-0FF) the data returned is from a previous transfer to the Transfer Register. No automatic clocking of the Transfer Register occurs. To read the actual counter value you must generate either a front panel or software Transfer Register clock which clocks all the Transfer Registers with new data. You could also use the 'Read on the Fly' address for that channel which would automatically clock the Transfer Register for just that one channel.

Read and Clear Channel N:

For a single read (D16/D32) to an address in this block (base+ 100-1FF) the data returned is from a previous transfer to the Transfer Register and the channel N counter is cleared.

Read Channel N 'On The Fly':

For a single read (D32 only) to an address in this block (base+ 200-2FF) the Transfer Register for channel N is clocked and the data is readout. Other channel Transfer Registers are not clocked.

Test Mode

The module has a Test Mode that can be enabled by group by writing to base+ 31C. This gates the front panel Test Clock and the software 'single pulse' into the selected group channels. The standard Count Enables must be true, Test Mode just switches the count input clock sources.

Reference Mode

A Reference clock that is programmable can be enabled into channel 1 instead of the normal channel 1 input.. Set up is from base+ 414. This allows channel 1 to be used for a time record.

Trigger Mode

The front panel Clock Out, Internal Gate Size Register (0x412) and Programmable Clock and Trigger Mode Register (0x410) make up a ‘Gate Generator’ subsection of the VS64. It can be used separately or as part of the VS64 Global Count Enable. In Trigger Modes the front panel Gate/Trig input is a trigger for the ‘gate generator’ section of the VS64. This trigger input or the software trigger (0x42E) start an internal gate which can be used as part of the Global Count Enable. The internal gate size is set using a programmable clock and a 16 bit Gate Size Register. Set up is from 0x410 and 0x412. The clock out connector can be either the generated gate or a pulse burst for the duration of the generated gate. See setup register at 0x410 and listed exceptions. In Trigger Modes the front panel Arm input can be used as a gate.

MEMORY MAP

Offset*	Type		Function
000-0FC	D16/D32 BLT32	R	Read Channel N Counter Transfer Register (no register clock) 000-003= Ch1, 0FC-0FF = Ch64
100-1FC	D16/D32	R	Read Channel N Counter Transfer Register & Clear Counter N (no register clock), 100-103= Ch1, 1FC-1FF = Ch64
200-2FC	D32	R	Read Channel N Counter 'On the FLY' (clock only Channel N Transfer Register) 200-203= Ch1, 2FC-2FF = Ch64
400	D16	R	Status Register (see tables that follow for specs)
402	D16	R/W	Control Register (see tables that follow for specs)
404	D16	R/W	A32 Base Address Register, A31-A16 (A16 access only)
406	D16	R/W	A32 Base Address Register, A15-A11 (A16 access only)
409	D08(O)	R/W	Interrupter #1 Status/ID Register (overflow)
40B	D08(O)	R/W	Interrupter #2 Status/ID Register (front panel transfer clock)
40D	D08(O)	R/W	Interrupter #3 Status/ID Register (end of gate)
40E	D16	R/W	Interrupter Set Up Register for 3 Interrupters
410	D16	R/W	Programmable Clock & Trigger Mode Register
412	D16	R/W	Internal Gate Size Register
414	D16	R/W	Programmable Reference Clock & Reference Mode Register
416	D16	R/W	A24 Base Address Register, A15-A11 (A16 access only)
41E	D16	R	ID Register, Module Type, Options and Serial Number
420	---	W	Master Reset (set all registers to default, like power up)
422	---	W	Clock All Counter Transfer Registers
424	---	W	Global Count Enable (readout in Status Register)
426	---	W	Global Count Disable
428	---	W	Global Reset (Counters and Overflows)
42A	---	W	ARM
42C	---	W	DISARM
42E	---	W	Trigger Internal Gate
430	---	W	Generate Single Test Pulse to test mode enabled groups
432	D16	W	Clear IRQ#2 and/or IRQ#3 Requests and Sources

*Offset (A10-A0) from Base address

NOTE: Selective = Do by Individual Channel
Group = Do by 16 Channel Group
Global =Do All Channels

Offset*	Type		Function
300- 33F	D16	R/W	Registers for Channels 1 - 16 and Group Access (see tables that follow for specs)
340- 37F	D16	R/W	Registers for Channels 17 - 32 (see tables that follow for specs)
380- 3BF	D16	R/W	Registers for Channels 33 - 48 (see tables that follow for specs)
3C0- 3FF	D16	R/W	Registers for Channels 49 - 64 (see tables that follow for specs)
300	D16	R/W	Selective Overflow Enable Register Channel 1-16
302	D16	R/W	Selective Overflow Reset Enable Register Channel 1-16
304	D16	R/W	Selective Counter Reset Enable Register Channel 1-16
306**	D16	R/W	Selective Count Enable Register Ch 1-16 (default to all enabled)
308	D16	R	Overflow Register Channel 1-16
30A	D16	R	Enabled Overflow Register Channel 1-16 (IRQ#1 source by Channel)
310	D16	W	Group Selective Overflow Reset, D0-D3 Select Ch Group(s)
312	D16	W	Group Overflow Reset, D0-D3 Select Channel Group(s)
314	D16	W	Group Selective Counter Reset, D0-D3 Select Channel Group(s)
316	D16	W	Group Counter Reset, D0-D3 Select Channel Group(s)
318**	D16	R/W	Group Selective Count Enable, D0-D3 Select Channel Group(s)
31A	D16	R/W	Group Overflow Enable, D0-D3 Select Channel Group(s)
31C	D16	R/W	Group Test Mode Enable, D0-D3 Select Channel Group(s)
31E	D16	R/W	Group Overflow Bit (24or32) Select, D0-D3 Select Ch Group(s)
340	D16	R/W	Selective Overflow Enable Register Channel 17 - 32
342	D16	R/W	Selective Overflow Reset Enable Register Channel 17 - 32
344	D16	R/W	Selective Counter Reset Enable Register Channel 17 - 32
346**	D16	R/W	Selective Count Enable Register Ch 17 - 32 (default to all enabled)
348	D16	R	Overflow Register Channel 17 - 32
34A	D16	R	Enabled Overflow Register Channel 17-32 (IRQ#1 source by Channel)
380	D16	R/W	Selective Overflow Enable Register Channel 33 - 48
382	D16	R/W	Selective Overflow Reset Enable Register Channel 33 - 48
384	D16	R/W	Selective Counter Reset Enable Register Channel 33 - 48
386**	D16	R/W	Selective Count Enable Register Ch 33 - 48 (default to all enabled)
388	D16	R	Overflow Register Channel 33 - 48
38A	D16	R	Enabled Overflow Register Channel 33-48 (IRQ#1 source by channel)
3C0	D16	R/W	Selective Overflow Enable Register Channel 49 - 64
3C2	D16	R/W	Selective Overflow Reset Enable Register Channel 49 - 64
3C4	D16	R/W	Selective Counter Reset Enable Register Channel 49 - 64
3C6**	D16	R/W	Selective Count Enable Register Ch 49 - 64 (default to all enabled)
3C8	D16	R	Overflow Register Channel 49 - 64
3CA	D16	R	Enabled Overflow Register Channel 49-64 (IRQ#1 source by channel)

NOTE: ** default is true (enabled)

STATUS REGISTER

Base + **400**H (A10-A0)

D15	NOT USED	
D14	NOT USED	
D13	NOT USED	
D12	1 = Front Panel Arm Output is True (asserting ARM)	READ ONLY
D11	1 = Front Panel Arm Input is True (asserting ARM)	READ ONLY
D10	1 = Front Panel Gate Input is True (asserting GATE OPEN)	READ ONLY
D9	1 = Programmed Internal Gate is True (asserting GATE OPEN)	READ ONLY
D8	1 = Front Panel Reset Input is True (asserting RESET)	READ ONLY
D7	1 = IRQ#3 Set (Gate has Ended)	READ ONLY
D6	1 = IRQ#2 Set (FP Clock Registers Received)	READ ONLY
D5	1 = IRQ#1 Set (Overflow has occurred)	READ ONLY
D4	1 = IRQ#3 Source Set (Gate has Ended)	READ ONLY
D3	1 = IRQ#2 Source Set (FP Transfer Clock Received)	READ ONLY
D2	1 = IRQ#1 Source Set (Overflow has occurred)	READ ONLY
D1	1 = Global Count Enable FF is ENABLED	READ ONLY
D0	1 = Global Count Enable is ENABLED	READ ONLY

CONTROL REGISTER

Base + **402**H (A10-A0)

D15	NOT USED	
D14	NOT USED	
D13	NOT USED	
D12	NOT USED	
D11	NOT USED	
D10	NOT USED	
D9	NOT USED	
D8	NOT USED	
D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	NOT USED	
D3	NOT USED	
D2	NOT USED	
D1	1 = Enable Global Counter Reset on Front Panel Transfer Register Clock	R/W
D0	1 = Enable Global Counter Reset on VME Transfer Register Clock	R/W

Note: The Transfer Register is Clocked then the Counters and Overflows are Reset.

A32 BASE ADDRESS REGISTER High

Base + **404**H (A10-A0)

D15	1 = A31 Added for A32 Base Address	R/W
D14	1 = A30 Added for A32 Base Address	R/W
D13	1 = A29 Added for A32 Base Address	R/W
D12	1 = A28 Added for A32 Base Address	R/W
D11	1 = A27 Added for A32 Base Address	R/W
D10	1 = A26 Added for A32 Base Address	R/W
D9	1 = A25 Added for A32 Base Address	R/W
D8	1 = A24 Added for A32 Base Address	R/W
D7	1 = A23 Added for A32 Base Address	R/W
D6	1 = A22 Added for A32 Base Address	R/W
D5	1 = A21 Added for A32 Base Address	R/W
D4	1 = A20 Added for A32 Base Address	R/W
D3	1 = A19 Added for A32 Base Address	R/W
D2	1 = A18 Added for A32 Base Address	R/W
D1	1 = A17 Added for A32 Base Address	R/W
D0	1 = A16 Added for A32 Base Address	R/W

A32 BASE ADDRESS REGISTER Low

Base + **406**H (A10-A0)

D15	NOT USED	
D14	NOT USED	
D13	NOT USED	
D12	NOT USED	
D11	NOT USED	
D10	NOT USED	
D9	NOT USED	
D8	NOT USED	
D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	1 = A15 Added for A32 Base Address	R/W
D3	1 = A14 Added for A32 Base Address	R/W
D2	1 = A13 Added for A32 Base Address	R/W
D1	1 = A12 Added for A32 Base Address	R/W
D0	1 = A11 Added for A32 Base Address	R/W

INTERRUPTER #1 STATUS/ID REGISTER (overflow)

Base + **408**H (A10-A0)

D7	IRQ ID Bit 7, Returned during VME IACK Cycle	R/W
D6	IRQ ID Bit 6, Returned during VME IACK Cycle	R/W
D5	IRQ ID Bit 5, Returned during VME IACK Cycle	R/W
D4	IRQ ID Bit 4, Returned during VME IACK Cycle	R/W
D3	IRQ ID Bit 3, Returned during VME IACK Cycle	R/W
D2	IRQ ID Bit 2, Returned during VME IACK Cycle	R/W
D1	IRQ ID Bit 1, Returned during VME IACK Cycle	R/W
D0	IRQ ID Bit 0, Returned during VME IACK Cycle	R/W

INTERRUPTER #2 STATUS/ID REGISTER (FP Transfer Clock)

Base + **40A**H (A10-A0)

D7	IRQ ID Bit 7, Returned during VME IACK Cycle	R/W
D6	IRQ ID Bit 6, Returned during VME IACK Cycle	R/W
D5	IRQ ID Bit 5, Returned during VME IACK Cycle	R/W
D4	IRQ ID Bit 4, Returned during VME IACK Cycle	R/W
D3	IRQ ID Bit 3, Returned during VME IACK Cycle	R/W
D2	IRQ ID Bit 2, Returned during VME IACK Cycle	R/W
D1	IRQ ID Bit 1, Returned during VME IACK Cycle	R/W
D0	IRQ ID Bit 0, Returned during VME IACK Cycle	R/W

INTERRUPTER #3 STATUS/ID REGISTER (End of Gate)

Base + **40C**H (A10-A0)

D7	IRQ ID Bit 7, Returned during VME IACK Cycle	R/W
D6	IRQ ID Bit 6, Returned during VME IACK Cycle	R/W
D5	IRQ ID Bit 5, Returned during VME IACK Cycle	R/W
D4	IRQ ID Bit 4, Returned during VME IACK Cycle	R/W
D3	IRQ ID Bit 3, Returned during VME IACK Cycle	R/W
D2	IRQ ID Bit 2, Returned during VME IACK Cycle	R/W
D1	IRQ ID Bit 1, Returned during VME IACK Cycle	R/W
D0	IRQ ID Bit 0, Returned during VME IACK Cycle	R/W

INTERRUPTER SETUP REGISTERS

Base + **40E**H (A10-A0)

D15	NOT USED		
D14	NOT USED		
D13	NOT USED		
D12	NOT USED		
D11	Interrupter #3 IRQ ENABLE (1 = enabled)	**End of Gate**	R/W
D10	Interrupter #3 Level Bit 2		R/W
D9	Interrupter #3 Level Bit 1		R/W
D8	Interrupter #3 Level Bit 0		R/W
D7	Interrupter #2 IRQ ENABLE (1 = enabled)	**FP Transfer Clock**	R/W
D6	Interrupter #2 Level Bit 2		R/W
D5	Interrupter #2 Level Bit 1		R/W
D4	Interrupter #2 Level Bit 0		R/W
D3	Interrupter #1 IRQ ENABLE (1 = enabled)	**Overflow**	R/W
D2	Interrupter #1 Level Bit 2		R/W
D1	Interrupter #1 Level Bit 1		R/W
D0	Interrupter #1 Level Bit 0		R/W

PROGRAMMABLE CLOCK & TRIGGER MODE REGISTER

Also Clock/Gate Generator to front panel Output connector

Base + **410**H (A10-A0)

D7-15	NOT USED	
D6	Front Panel Clock Out: 0=Pulses 1=Internal Gate(Trig Mode)	R/W
D5	Trigger Mode Select bit 2	R/W
D4	Trigger Mode Select bit 1	R/W
D3	Programmable Clock Frequency Select Bit 3	R/W
D2	Programmable Clock Frequency Select Bit 2	R/W
D1	Programmable Clock Frequency Select Bit 1	R/W
D0	Programmable Clock Frequency Select Bit 0	R/W

	BIT 0-3	Clock Frequency	Period (**T**)
	0	10MHz (DEFAULT)	100 ns
*	1	50MHz	20 ns
	2	25MHz	40 ns
	3	5MHz	200 ns
	4	2.5MHz	400 µs
	5	1MHz	1 µs
	6	500KHz	2 µs
	7	250KHz	4 µs
	8	100KHz	10 µs
	9	50KHz	20 µs
	10	25KHz	40 µs
	11	10KHz	100 µs
	12	1KHz	1 ms
	13	100Hz	10 ms
	14	not used	
*	15	Channel 1 Input	

BIT 4-5	Trig Mode Actions
0	No Internal Gate, Clock Out is continuous selected clock
1	Internal Gate used as Global Gate, FP Gate/Trig input is Trigger, Clock Out is gated clock or Internal Gate as selected by D6 (see above)
2	Internal Gate NOT used as Global Gate (Arm In can be used as Gate if needed), FP Gate/Trig input is Trigger, Clock Out is gated clock or Internal Gate as selected by D6 (see above) Looks like stand alone Gate/Pulse Generator, NO interaction with rest of card.
3	NOT USED

* For 50Mhz clock & Ch 1 Input selections the Pulse output is not useable in Trigger Mode
The selected clock frequency is normally available at the front panel 'Clock Out' connector as a continuous clock. For Trigger Modes the 'Clock Out' is a gated clock burst for the duration of the internally generated gate or the Internal Gate itself as selected above.

INTERNAL GATE SIZE REGISTER

Base + **412**H (A10-A0)

D15	1= 32768 periods	R/W
D14	1= 16384 periods	R/W
D13	1= 8092 periods	R/W
D12	1= 4096 periods	R/W
D11	1= 2048 periods	R/W
D10	1= 1024 periods	R/W
D9	1= 512 periods	R/W
D8	1= 256 periods	R/W
D7	1= 128 periods	R/W
D6	1= 64 periods	R/W
D5	1= 32 periods	R/W
D4	1= 16 periods	R/W
D3	1= 8 periods	R/W
D2	1= 4 periods	R/W
D1	1= 2 periods	R/W
D0	1= 1 period	R/W

Note: Recommended minimum Gate Size of 4

To calculate Gate Size add values of selected bits, add 1 and multiply by the Period (T) of the Selected Clock

The Internal Gate starts approximately 23ns after the FP Trigger In down edge plus 0 - 20ns of jitter to synchronize the Trigger to the internal clock. This time is constant no matter which clock is selected (except from CH1-Sig Input). A software trigger is also provided, see base+42E.

During the Internal Gate Time the front panel Clock Out signal is a pulse train at the selected frequency containing the total selected bits above plus 2 additional pulses, all pulses are fully formed. The first pulse is approximately 3ns before the Internal Gate starts. See exceptions listed under base+410 tables.

If D6 = 1 for base+410, front panel Clock Out signal is the Internal Gate.

PROGRAMMABLE REFERENCE CLOCK REGISTER

Base + **414**H (A10-A0)

D15	NOT USED	
D14	NOT USED	
D13	NOT USED	
D12	NOT USED	
D11	NOT USED	
D10	NOT USED	
D9	NOT USED	
D8	NOT USED	
D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	NOT USED	
D3	Enable Reference Clock (1 = Ref Clock enabled into Channel 1)	R/W
D2	Reference Clock Frequency Select Bit 2	R/W
D1	Reference Clock Frequency Select Bit 1	R/W
D0	Reference Clock Frequency Select Bit 0	R/W

BIT 0-2	Reference Clock Frequency
0	50MHz (DEFAULT)
1	25MHz
2	10MHz
3	5MHz
4	2.5MHz
5	1MHz
6	500KHz
7	100KHz

BROADCAST COMMAND SETUP REGISTER

(set A24 base address and Enable Broadcast participation)

Base + **416**H (A10-A0)

D9	1 = Enable Broadcast Participation	R/W
D8	1 = Master (0 = Slave)	R/W
D7	1 = A23 Added for A24 Base Address	R/W
D6	1 = A22 Added for A24 Base Address	R/W
D5	1 = A21 Added for A24 Base Address	R/W
D4	1 = A20 Added for A24 Base Address	R/W
D3	1 = A19 Added for A24 Base Address	R/W
D2	1 = A18 Added for A24 Base Address	R/W
D1	1 = A17 Added for A24 Base Address	R/W
D0	1 = A16 Added for A24 Base Address	R/W

MODULE ID REGISTER

Base + **41E**H (A10-A0)

D15	Module Type &Options Bit 5	READ ONLY
D14	Module Type &Options Bit 4	READ ONLY
D13	Module Type &Options Bit 3	READ ONLY
D12	Module Type &Options Bit 2	READ ONLY
D11	Module Type &Options Bit 1	READ ONLY
D10	Module Type &Options Bit 0	READ ONLY
D9	Serial Number Bit 9	READ ONLY
D8	Serial Number Bit 8	READ ONLY
D7	Serial Number Bit 7	READ ONLY
D6	Serial Number Bit 6	READ ONLY
D5	Serial Number Bit 5	READ ONLY
D4	Serial Number Bit 4	READ ONLY
D3	Serial Number Bit 3	READ ONLY
D2	Serial Number Bit 2	READ ONLY
D1	Serial Number Bit 1	READ ONLY
D0	Serial Number Bit 0	READ ONLY

BIT 10-15	Module Type & Options
0	not used
1	VTR1012A
2	VTR3012A
3	VTR10010
4	VWG
5	VTR812
6	VTR812/40
7 - 15	not used
16	VS64 (TTL)
17	VS32 (TTL)
18	VS16 (TTL)
19	VS32 (ECL)
20	VS16 (ECL)
21	VS32 (NIM)
22	VS16 (NIM)
23	VS64D (TTL)
24	VS32D (TTL)
25	VS16D (TTL)
26	VS32D (ECL)
27	VS16D (ECL)
28	VS32D (NIM)
29	VS16D (NIM)
30 - 63	not used

MASTER RESET

Base + **420**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

complete module Reset, same as SYSRESET or Power up

Sets all registers to default, counters to zero and aborts any cycle.

CLOCK TRANSFER REGISTERS

Base + **422**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Clock all counter Transfer Registers, same as front panel Transfer Clock

If bit D0 in Control Register is set, all counters will be cleared after the transfer

GLOBAL COUNT ENABLE

Base + **424**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Sets Global Enable Bit (Bit which is 'ANDed' with every channels individual enable)

Read status in Status Register, bit D1

GLOBAL COUNT DISABLE

Base + **426**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Clears Global Enable Bit (Bit which is 'ANDed' with every channels individual enable)

Read status in Status Register, bit D1

GLOBAL RESET of COUNTERS

Base + **428**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Clears counter and overflow for all channels and Clears Overflow IRQ Source

ARM

Base + **42A**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Sets front panel 'ARM OUT' to 1 (armed)

Read status in Status Register, bit D12

DISARM

Base + **42C**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Sets front panel 'ARM OUT' to 0 (disarmed, default state)

Read status in Status Register, bit D12

TRIGGER INTERNAL GATE

Base + **42E**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Starts Internal Gate if Mode is set to 'Trigger Mode'(see base + 410)

Also starts FP Clock/Gate Out

TEST PULSE

Base + **430**H (A10-A0) (DS0=1) BYTE 1

Write only Data ignored

Generate a Single Test Pulse to channel groups which are enabled for Test Mode (see base + 31C)

CLEAR IRQ REQUESTS and SOURCES

Base + **432**H (A10-A0) (DS0=1) BYTE 1

D1*	1 = Clear IRQ#3 Source (Gate End)	WRITE ONLY
D0*	1 = Clear IRQ#2 Source (FP Transfer Clock Received)	WRITE ONLY
IRQ#1 Source (Overflow)	Each participating channel overflow must be cleared or disabled since the IRQ source is the 'OR' of all enabled overflow bits.	

* Removes IRQ from VME Bus also.

IRQ#2 and IRQ#3 are also cleared and removed from bus when their Status/ID is readout during an IACK cycle (ROAK interrupters).

NOTE: Selective = Do by Individual Channel
Group = Do by 16 Channel Group
Global =Do All Channels

SELECTIVE OVERFLOW ENABLE REGISTERS for CHANNEL GROUPS

Base + **300**H GROUP 1 (Ch 1-16)
Base + **340**H GROUP 2 (Ch 17-32)
Base + **380**H GROUP 3 (Ch 33-48)
Base + **3C0**H GROUP 4 (Ch 49-64)

D15	1 = Enable group channel 16 overflow into 'OR' for Group Overflow	R/W
D14	1 = Enable group channel 15 overflow into 'OR' for Group Overflow	R/W
D13	1 = Enable group channel 14 overflow into 'OR' for Group Overflow	R/W
D12	1 = Enable group channel 13 overflow into 'OR' for Group Overflow	R/W
D11	1 = Enable group channel 12 overflow into 'OR' for Group Overflow	R/W
D10	1 = Enable group channel 11 overflow into 'OR' for Group Overflow	R/W
D9	1 = Enable group channel 10 overflow into 'OR' for Group Overflow	R/W
D8	1 = Enable group channel 9 overflow into 'OR' for Group Overflow	R/W
D7	1 = Enable group channel 8 overflow into 'OR' for Group Overflow	R/W
D6	1 = Enable group channel 7 overflow into 'OR' for Group Overflow	R/W
D5	1 = Enable group channel 6 overflow into 'OR' for Group Overflow	R/W
D4	1 = Enable group channel 5 overflow into 'OR' for Group Overflow	R/W
D3	1 = Enable group channel 4 overflow into 'OR' for Group Overflow	R/W
D2	1 = Enable group channel 3 overflow into 'OR' for Group Overflow	R/W
D1	1 = Enable group channel 2 overflow into 'OR' for Group Overflow	R/W
D0	1 = Enable group channel 1 overflow into 'OR' for Group Overflow	R/W

NOTE: See base + 31A for Group Overflow Commands that use these registers

SELECTIVE OVERFLOW RESET ENABLE REGISTERS for CHANNEL GROUPS

Base + **302**H GROUP 1 (Ch 1-16)
Base + **342**H GROUP 2 (Ch 17-32)
Base + **382**H GROUP 3 (Ch 33-48)
Base + **3C2**H GROUP 4 (Ch 49-64)

D15	1 = Enable group channel 16 Overflow Reset for Group Overflow Reset	R/W
D14	1 = Enable group channel 15 Overflow Reset for Group Overflow Reset	R/W
D13	1 = Enable group channel 14 Overflow Reset for Group Overflow Reset	R/W
D12	1 = Enable group channel 13 Overflow Reset for Group Overflow Reset	R/W
D11	1 = Enable group channel 12 Overflow Reset for Group Overflow Reset	R/W
D10	1 = Enable group channel 11 Overflow Reset for Group Overflow Reset	R/W
D9	1 = Enable group channel 10 Overflow Reset for Group Overflow Reset	R/W
D8	1 = Enable group channel 9 Overflow Reset for Group Overflow Reset	R/W
D7	1 = Enable group channel 8 Overflow Reset for Group Overflow Reset	R/W
D6	1 = Enable group channel 7 Overflow Reset for Group Overflow Reset	R/W
D5	1 = Enable group channel 6 Overflow Reset for Group Overflow Reset	R/W
D4	1 = Enable group channel 5 Overflow Reset for Group Overflow Reset	R/W
D3	1 = Enable group channel 4 Overflow Reset for Group Overflow Reset	R/W
D2	1 = Enable group channel 3 Overflow Reset for Group Overflow Reset	R/W
D1	1 = Enable group channel 2 Overflow Reset for Group Overflow Reset	R/W
D0	1 = Enable group channel 1 Overflow Reset for Group Overflow Reset	R/W

NOTE: See base + 310 for Group Overflow Reset Commands that use these registers

SELECTIVE COUNTER RESET ENABLE REGISTERS for CHANNEL GROUPS

Base + **304**H GROUP 1 (Ch 1-16)
Base + **344**H GROUP 2 (Ch 17-32)
Base + **384**H GROUP 3 (Ch 33-48)
Base + **3C4**H GROUP 4 (Ch 49-64)

D15	1 = Enable group channel 16 Counter Reset for Group Counter Reset	R/W
D14	1 = Enable group channel 15 Counter Reset for Group Counter Reset	R/W
D13	1 = Enable group channel 14 Counter Reset for Group Counter Reset	R/W
D12	1 = Enable group channel 13 Counter Reset for Group Counter Reset	R/W
D11	1 = Enable group channel 12 Counter Reset for Group Counter Reset	R/W
D10	1 = Enable group channel 11 Counter Reset for Group Counter Reset	R/W
D9	1 = Enable group channel 10 Counter Reset for Group Counter Reset	R/W
D8	1 = Enable group channel 9 Counter Reset for Group Counter Reset	R/W
D7	1 = Enable group channel 8 Counter Reset for Group Counter Reset	R/W
D6	1 = Enable group channel 7 Counter Reset for Group Counter Reset	R/W
D5	1 = Enable group channel 6 Counter Reset for Group Counter Reset	R/W
D4	1 = Enable group channel 5 Counter Reset for Group Counter Reset	R/W
D3	1 = Enable group channel 4 Counter Reset for Group Counter Reset	R/W
D2	1 = Enable group channel 3 Counter Reset for Group Counter Reset	R/W
D1	1 = Enable group channel 2 Counter Reset for Group Counter Reset	R/W
D0	1 = Enable group channel 1 Counter Reset for Group Counter Reset	R/W

NOTE: See base + 316 for Group Counter Reset Commands that use these registers
Counter Resets also clear corresponding Overflow

SELECTIVE COUNT ENABLE REGISTERS for CHANNEL GROUPS

Base + **306**H GROUP 1 (Ch 1-16)
Base + **346**H GROUP 2 (Ch 17-32)
Base + **386**H GROUP 3 (Ch 33-48)
Base + **3C6**H GROUP 4 (Ch 49-64)

D15	1 = Enable group channel 16 Count Enable for Group Selective Count Enable	R/W
D14	1 = Enable group channel 15 Count Enable for Group Selective Count Enable	R/W
D13	1 = Enable group channel 14 Count Enable for Group Selective Count Enable	R/W
D12	1 = Enable group channel 13 Count Enable for Group Selective Count Enable	R/W
D11	1 = Enable group channel 12 Count Enable for Group Selective Count Enable	R/W
D10	1 = Enable group channel 11 Count Enable for Group Selective Count Enable	R/W
D9	1 = Enable group channel 10 Count Enable for Group Selective Count Enable	R/W
D8	1 = Enable group channel 9 Count Enable for Group Selective Count Enable	R/W
D7	1 = Enable group channel 8 Count Enable for Group Selective Count Enable	R/W
D6	1 = Enable group channel 7 Count Enable for Group Selective Count Enable	R/W
D5	1 = Enable group channel 6 Count Enable for Group Selective Count Enable	R/W
D4	1 = Enable group channel 5 Count Enable for Group Selective Count Enable	R/W
D3	1 = Enable group channel 4 Count Enable for Group Selective Count Enable	R/W
D2	1 = Enable group channel 3 Count Enable for Group Selective Count Enable	R/W
D1	1 = Enable group channel 2 Count Enable for Group Selective Count Enable	R/W
D0	1 = Enable group channel 1 Count Enable for Group Selective Count Enable	R/W

NOTE: See base + 318for Group Selective Count Enable Commands that use these registers
This register defaults to all 1's for Sysreset, Master Reset and Power up

OVERFLOW REGISTERS for CHANNEL GROUPS

Base + **308**H GROUP 1 (Ch 1-16)
Base + **348**H GROUP 2 (Ch 17-32)
Base + **388**H GROUP 3 (Ch 33-48)
Base + **3C8**H GROUP 4 (Ch 49-64)

D15	1 = group channel 16 Overflow	READ ONLY
D14	1 = group channel 15 Overflow	READ ONLY
D13	1 = group channel 14 Overflow	READ ONLY
D12	1 = group channel 13 Overflow	READ ONLY
D11	1 = group channel 12 Overflow	READ ONLY
D10	1 = group channel 11 Overflow	READ ONLY
D9	1 = group channel 10 Overflow	READ ONLY
D8	1 = group channel 9 Overflow	READ ONLY
D7	1 = group channel 8 Overflow	READ ONLY
D6	1 = group channel 7 Overflow	READ ONLY
D5	1 = group channel 6 Overflow	READ ONLY
D4	1 = group channel 5 Overflow	READ ONLY
D3	1 = group channel 4 Overflow	READ ONLY
D2	1 = group channel 3 Overflow	READ ONLY
D1	1 = group channel 2 Overflow	READ ONLY
D0	1 = group channel 1 Overflow	READ ONLY

ENABLED OVERFLOW REGISTERS for CHANNEL GROUPS

Base + **30A**H GROUP 1 (Ch 1-16)
Base + **34A**H GROUP 2 (Ch 17-32)
Base + **38A**H GROUP 3 (Ch 33-48)
Base + **3CA**H GROUP 4 (Ch 49-64)

D15	1 = group channel 16 Enabled Overflow	READ ONLY
D14	1 = group channel 15 Enabled Overflow	READ ONLY
D13	1 = group channel 14 Enabled Overflow	READ ONLY
D12	1 = group channel 13 Enabled Overflow	READ ONLY
D11	1 = group channel 12 Enabled Overflow	READ ONLY
D10	1 = group channel 11 Enabled Overflow	READ ONLY
D9	1 = group channel 10 Enabled Overflow	READ ONLY
D8	1 = group channel 9 Enabled Overflow	READ ONLY
D7	1 = group channel 8 Enabled Overflow	READ ONLY
D6	1 = group channel 7 Enabled Overflow	READ ONLY
D5	1 = group channel 6 Enabled Overflow	READ ONLY
D4	1 = group channel 5 Enabled Overflow	READ ONLY
D3	1 = group channel 4 Enabled Overflow	READ ONLY
D2	1 = group channel 3 Enabled Overflow	READ ONLY
D1	1 = group channel 2 Enabled Overflow	READ ONLY
D0	1 = group channel 1 Enabled Overflow	READ ONLY

GROUP SELECTIVE OVERFLOW RESET

Base + **310**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Reset Selected Overflows (base+3C2) for GROUP 4 (Channels 49-64)	W
D2	1 = Reset Selected Overflows (base+382) for GROUP 3 (Channels 33-48)	W
D1	1 = Reset Selected Overflows (base+342) for GROUP 2 (Channels 17-32)	W
D0	1 = Reset Selected Overflows (base+302) for GROUP 1 (Channels 1-16)	W

GROUP OVERFLOW RESET

Base + **312**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Reset All Overflows for GROUP 4 (Channels 49-64)	W
D2	1 = Reset All Overflows for GROUP 3 (Channels 33-48)	W
D1	1 = Reset All Overflows for GROUP 2 (Channels 17-32)	W
D0	1 = Reset All Overflows for GROUP 1 (Channels 1-16)	W

GROUP SELECTIVE COUNTER RESET

Base + **314**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Reset Selected Counters (base+3C4) for GROUP 4 (Channels 49-64)	W
D2	1 = Reset Selected Counters (base+384) for GROUP 3 (Channels 33-48)	W
D1	1 = Reset Selected Counters (base+344) for GROUP 2 (Channels 17-32)	W
D0	1 = Reset Selected Counters (base+304) for GROUP 1 (Channels 1-16)	W

GROUP COUNTER RESET

Base + **316**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Reset All Counters for GROUP 4 (Channels 49-64)	W
D2	1 = Reset All Counters for GROUP 3 (Channels 33-48)	W
D1	1 = Reset All Counters for GROUP 2 (Channels 17-32)	W
D0	1 = Reset All Counters for GROUP 1 (Channels 1-16)	W

GROUP SELECTIVE COUNT ENABLE

Base + **318**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Enable Selected Counters (base+3C6) for GROUP 4 (Channels 49-64)	R/W
D2	1 = Enable Selected Counters (base+386) for GROUP 3 (Channels 33-48)	R/W
D1	1 = Enable Selected Counters (base+346) for GROUP 2 (Channels 17-32)	R/W
D0	1 = Enable Selected Counters (base+306) for GROUP 1 (Channels 1-16)	R/W

GROUP OVERFLOW ENABLE

Base + **31A**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Enable Selected Overflows (base+3C0) for GROUP 4 (Channels 49-64)	R/W
D2	1 = Enable Selected Overflows (base+380) for GROUP 3 (Channels 33-48)	R/W
D1	1 = Enable Selected Overflows (base+340) for GROUP 2 (Channels 17-32)	R/W
D0	1 = Enable Selected Overflows (base+300) for GROUP 1 (Channels 1-16)	R/W

GROUP TEST MODE ENABLE

Base + **31C**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Test Mode Enabled for GROUP 4 (Channels 49-64)	R/W
D2	1 = Test Mode Enabled for GROUP 3 (Channels 33-48)	R/W
D1	1 = Test Mode Enabled for GROUP 2 (Channels 17-32)	R/W
D0	1 = Test Mode Enabled for GROUP 1 (Channels 1-16)	R/W

GROUP OVERFLOW BIT (24or32) SELECT

Base + **31E**H (A10-A0) (DS0=1) BYTE 1

D4-D15	Not-used	
D3	1 = Overflow from Bit 24 (0=Bit 32) for GROUP 4 (Channels 49-64)	R/W
D2	1 = Overflow from Bit 24 (0=Bit 32) for GROUP 3 (Channels 33-48)	R/W
D1	1 = Overflow from Bit 24 (0=Bit 32) for GROUP 2 (Channels 17-32)	R/W
D0	1 = Overflow from Bit 24 (0=Bit 32) for GROUP 1 (Channels 1-16)	R/W

Trailing edge of bit 24 or 32 is used

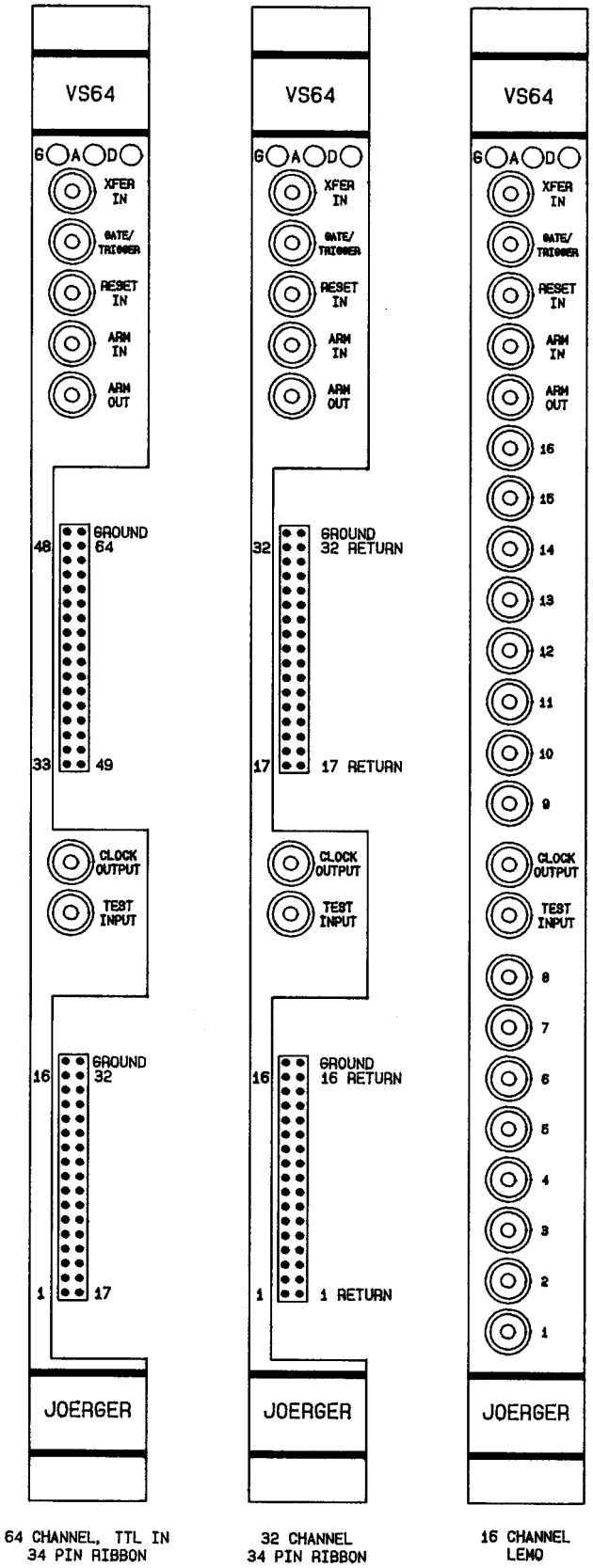
NOTE: Selective = Do by Individual Channel
Group = Do by 16 Channel Group
Global =Do All Channels

FRONT PANEL LAYOUTS

G = **Module is Active**
(Global Count Enable is True)

A = **Module is Armed**
(front panel Arm In = True)

D = **Module Addressed via VME**
bus **(Dtack=True)**



64 CHANNEL, TTL IN
34 PIN RIBBON

32 CHANNEL
34 PIN RIBBON

16 CHANNEL
LEMO

JOERGER ENTERPRISES, INC.
MODEL VS64
64 CHANNEL TTL INPUT
CONNECTOR: 34 PIN , AMP TYPE 499709-8

GROUND	34	33	GROUND
INPUT 48	32	31	INPUT 64
INPUT 47	30	29	INPUT 63
INPUT 46	28	27	INPUT 62
INPUT 45	26	25	INPUT 61
INPUT 44	24	23	INPUT 60
INPUT 43	22	21	INPUT 59
INPUT 42	20	19	INPUT 58
INPUT 41	18	17	INPUT 57
INPUT 40	16	15	INPUT 56
INPUT 39	14	13	INPUT 55
INPUT 38	12	11	INPUT 54
INPUT 37	10	9	INPUT 53
INPUT 36	8	7	INPUT 52
INPUT 35	6	5	INPUT 51
INPUT 34	4	3	INPUT 50
INPUT 33	2	1	INPUT 49

CABLE SHOULD EXIT FROM THIS SIDE OF CONNECTOR

GROUND	34	33	GROUND
INPUT 16	32	31	INPUT 32
INPUT 15	30	29	INPUT 31
INPUT 14	28	27	INPUT 30
INPUT 13	26	25	INPUT 29
INPUT 12	24	23	INPUT 28
INPUT 11	22	21	INPUT 27
INPUT 10	20	19	INPUT 26
INPUT 9	18	17	INPUT 25
INPUT 8	16	15	INPUT 24
INPUT 7	14	13	INPUT 23
INPUT 6	12	11	INPUT 22
INPUT 5	10	9	INPUT 21
INPUT 4	8	7	INPUT 20
INPUT 3	6	5	INPUT 19
INPUT 2	4	3	INPUT 18
INPUT 1	2	1	INPUT 17

CABLE SHOULD EXIT FROM THIS SIDE OF CONNECTOR

STANDARD TTL INPUT, NEGATIVE GOING SIGNAL, 1KΩ PULL UP TO +5V
OPTIONAL TTL INPUT, POSITIVE GOING SIGNAL, 50Ω TO GROUND

JOERGER ENTERPRISES, INC.
MODEL VS64
32 CHANNEL TTL ECL OR NIM INPUTS
CONNECTOR: 34 PIN , AMP TYPE 499709-8

GROUND	34	33	GROUND
INPUT 32	32	31	GROUND
INPUT 31	30	29	GROUND
INPUT 30	28	27	GROUND
INPUT 29	26	25	GROUND
INPUT 28	24	23	GROUND
INPUT 27	22	21	GROUND
INPUT 26	20	19	GROUND
INPUT 25	18	17	GROUND
INPUT 24	16	15	GROUND
INPUT 23	14	13	GROUND
INPUT 22	12	11	GROUND
INPUT 21	10	9	GROUND
INPUT 20	8	7	GROUND
INPUT 19	6	5	GROUND
INPUT 18	4	3	GROUND
INPUT 17	2	1	GROUND

CABLE SHOULD EXIT FROM THIS SIDE OF CONNECTOR

GROUND	34	33	GROUND
INPUT 16	32	31	GROUND
INPUT 15	30	29	GROUND
INPUT 14	28	27	GROUND
INPUT 13	26	25	GROUND
INPUT 12	24	23	GROUND
INPUT 11	22	21	GROUND
INPUT 10	20	19	GROUND
INPUT 9	18	17	GROUND
INPUT 8	16	15	GROUND
INPUT 7	14	13	GROUND
INPUT 6	12	11	GROUND
INPUT 5	10	9	GROUND
INPUT 4	8	7	GROUND
INPUT 3	6	5	GROUND
INPUT 2	4	3	GROUND
INPUT 1	2	1	GROUND

CABLE SHOULD EXIT FROM THIS SIDE OF CONNECTOR

STANDARD TTL INPUT, NEGATIVE GOING SIGNAL, 1KΩ PULL UP TO +5V
OPTIONAL TTL INPUT, POSITIVE GOING SIGNAL, 50Ω TO GROUND

JOERGER ENTERPRISES, INC.
MODEL VS64
REAR ACCESS (P2) TTL INPUT OPTION

Signal	Row C	Row A	Signal
INPUT 32	1	1	GROUND
INPUT 31	2	2	GROUND
INPUT 30	3	3	GROUND
INPUT 29	4	4	GROUND
INPUT 28	5	5	GROUND
INPUT 27	6	6	GROUND
INPUT 26	7	7	GROUND
INPUT 25	8	8	GROUND
INPUT 24	9	9	GROUND
INPUT 23	10	10	GROUND
INPUT 22	11	11	GROUND
INPUT 21	12	12	GROUND
INPUT 20	13	13	GROUND
INPUT 19	14	14	GROUND
INPUT 18	15	15	GROUND
INPUT 17	16	16	GROUND
INPUT 16	17	17	GROUND
INPUT 15	18	18	GROUND
INPUT 14	19	19	GROUND
INPUT 13	20	20	GROUND
INPUT 12	21	21	GROUND
INPUT 11	22	22	GROUND
INPUT 10	23	23	GROUND
INPUT 9	24	24	GROUND
INPUT 8	25	25	GROUND
INPUT 7	26	26	GROUND
INPUT 6	27	27	GROUND
INPUT 5	28	28	GROUND
INPUT 4	29	29	GROUND
INPUT 3	30	30	GROUND
INPUT 2	31	31	GROUND
INPUT 1	32	32	GROUND

STANDARD TTL INPUT, NEGATIVE GOING SIGNAL, 1KΩ PULL UP TO +5V
OPTIONAL TTL INPUT, POSITIVE GOING SIGNAL, 50Ω TO GROUND

INDEX

NOTES:

Rev-B, 11/06/02