	8GATE3
	9GATE4
	10GATE5
	11F1 - Internal 4Mhz
	12F2 - F1 / 16
	13F3 - F2 / 16
	14F4 - F3 / 16
	15F5 - F4 / 16
ECR	If CLKS is external, this specifies the clock rate.

1.4.2 Device Support routines

Device support consists of the following routines:

init_record(precord)

This routine checks to see if the card desired is present. If so it marks the associated channels used.

cmd(precord)

The following commands are accepted.

1.4 pulseTrainRecord

This device support module generates a pulse train. The user specifies the period and duty cycle. From these values the delay between the end of one pulse and the beginning of the next is computed as well as the pulse width.

Two Am9513 internal registers are used. The first is loaded with the number of clock ticks for the delay and the second the number for the pulse width. Since both registers contain unsigned 16 bit values the combination of the clock source, delay value, and pulse width puts a limit of the accuracy of the actual delay and pulse width. The actual delay and pulse width will always be an integral multiple of the clock rate and each must also be <=65535. Note that if CTYP is chosen to be internal then the optimal internal clock is automatically selected.

1.4.1 Field Used by Device Support

OUT Output Link

This must be a VME link. The signal number specifies a (chip,channel) combination as specified in the introduction to this chapter. Note that this also specifies the output signal.

LLOW Low logic level for output signal.

UNITS The time units (seconds, milliseconds, microseconds, nanoseconds, picoseconds).

PER Pulse train period in UNITS.

DCY Percent of time that signal is high.

GTYP Gate Type. (hardware, software). If GTYP is internal then HGV determines gating control.

HGV If GTYP is internal then this field can be set as follows:
0No Gating
1Active High Terminal Count from previous counter. Note that this is meaningless if signal is 0 or 5.
2Active high level GATE N+1, i.e., if this is counter N of a chip, counting will occur only while the gate input for couter N+1 is high.
3Active high level GATE N-1.
4Active high level GATE N.
5Active low level GATE N.

CEDG Clock signal edge. (0,1) forces counting on (leading, falling) edge of clock signal.

ECS External clock source. If CTYP is internal this field is ignored. If CTYP is external then this field can be set as follows:
0TCN-1. You probably do not want this.
1SRC1
2SRC2
3SRC3
4SRC4
5SRC5
6GATE1
7GATE2

	12F2 - F1 / 16
	13F3 - F2 / 16
	14F4 - F3 / 16
	15F5 - F4 / 16
ECR	Clock rate for external clock source.

1.3.2 Device Support routines

Device support consists of the following routines:

init_record(precord)

This routine checks to see if the card desired is present. If so it marks the associated channel used.

write(precord)

This command configures the associated signal.

1.3 pulseDelayRecord

The mz8310 is configured to look for a hardware or software trigger. A single delayed pulse is generated after each trigger.

Two Am9513 internal registers are used. The first is loaded with the number of clock ticks for the delay and the second the number for the pulse width. Since both registers contain unsigned 16 bit values the combination of the clock source, delay value, and pulse width puts a limit of the accuracy of the actual delay and pulse width. The actual delay and pulse width will always be an integral multiple of the clock rate and each must also be <=65535. Note that if CTYP is chosen to be internal then the optimal internal clock is automatically selected.

1.3.1 Field Used by Device Support

OUT	Output Link This must be a VME link. The signal number specifies a (chip,channel) combination as specified in the introduction to this chapter. Note that this also specifies the gate source and the output signal.
LLOW	Low logic level for output signal.
PFLD	Process Field. Indicates if DLY, WIDE, GATE, STV changed.
TTYP	Trigger Type (Hardware/Software). If hardware, then counter is set to use mode L (hardware triggered one shot), else it uses mode G (software triggered one-shot).
HTS	Hardware Trigger Source. (0,1) causes triggering on (leading,falling) edge. 0Leading edge 1Falling edge
STV	Soft Trigger Value. (Enable/Disable). This field will act as a trigger for the delay pulse when TTYP in Software (mode G).
GATE	Gate for pulse generation. Enable/Disable the generation of pulses.
UNITS	Time units.
DLY	Delay in UNITS after trigger edge until beginning of pulse.
WIDE	Width of pulse generated in UNITS.
CEDG	Clock edge. (0,1) forces counting on (leading, falling) edge of source signal.
ECS	External clock source. If CTYP is internal this field is ignored. If CTYP is external then this field can be set as follows: 0TCN-1. You probably do not want this. 1SRC1 2SRC2 3SRC3 4SRC4 5SRC5 6GATE1 7GATE2 8GATE3 9GATE4 10GATE5 11F1 - Internal 4Mhz

1.2.2 Device Support routines

Device support consists of the following routines:

init_record(precord)

This routine checks to see if the card desired is present. If so it marks the associated channels used.

cmd(precord)

The following commands are accepted.:

READ	This command reads the current value of the am9513 counters and places the value in VAL.
CLEAR	Clear the am9513 counters. Note that the counter is also stopped. The START command must be issued to restart the counter.
START	Start counting.
STOP	Stop the counter.
SETUP	Setup the am9513 to prepare for counting. Counting will not begin until the START command is issued.

1.2 pulseCounterRecord

The device support for pulseCounter records counts signal source pulses. The fields GTYP and HGV can be used to gate the source pulses.

1.2.1 Field Used by Device Support

VAL — Value Field

The read command places the current value of the counter in VAL.

OUT — Output Link

This must be a VME link. The signal corresponds to the first of two channels that will be used as a 32 bit unsigned counter. Thus signal and signal+1 are both used. Signal must not be 4 or 9.

GTYP — Gate Type. (hardware, software). If GTYP is internal then HGV determines gating control.

HGV — Internal Gate value. If GTYP is hardware then this field can be set as follows:
0No Gating
1Active High Terminal Count from previous counter. Note that this is meaningless if signal is 0 or 5.
2Active high level GATE N+1, i.e., if this is counter N of a chip, counting will occur only while the gate input for couter N+1 is high.
3Active high level GATE N-1.
4Active high level GATE N.
5Active low level GATE N.

CSIZ — Size of counter, 16 or 32 bit.

CNTE — Counter edge. (0,1) forces counting on (leading, falling) edge of source signal.

CNTS — Count source. This field can be set as follows:
0TCN-1. You probably do not want this.
1SRC1
2SRC2
3SRC3
4SRC4
5SRC5
6GATE1
7GATE2
8GATE3
9GATE4
10GATE5
11F1 - Internal 4Mhz
12F2 - F1 / 16
13F3 - F2 / 16
14F4 - F3 / 16
15F5 - F4 / 16

1.1 eventRecord

Each mz8310 module supports four seperate interrupts. When configuring INP signal (0,1,2,3) refers to interrupt (A,B,C,D).

In order to use interrupts jumpers K1, K2, K3, K4, and K6 must be configured properly. The configuration is as follows:

K1 This can be set so that you use the interrupt source desired.

K2 Same as K1

NOTE: K1 refers to signal for chip 2, i.e. 2O1, 2O2, etc. K2 refers to signals for chip 1. Note that the older versions of the Mizar manual are WRONG!!!!

K3 Jumper 3-4,5-6,11-12,15-16

K4 Jumper 1-2

K6 Jumper IRQA-IRQ1, IRQB-IRQ3, IRQC-IRQ5, IRQD-IRQ6

report(FILE fp)

This routine plays the same role as the report entry of a driver support module, i.e. it prints a report of all mz8310 modules.

init()

This routine is called once during IOC initialization. It looks for all mz8310 modules residing in the VME crate.

1 MIZAR MZ8310

The mz8310 device support module provides support for the following record types: event, pulseCounter, pulseDelay, and pulseTrain. No driver support is needed. Up to 4 mz8310 modules are supported. Each 8310 module contains 10 channels, which are identified as signals 0,...9. Each channel is individually configurable. Each mz8310 has two Am9513 Timing Controller chips. Each Am9513 has 5 counters. The relation between signal number, chip, counter, etc. is as follows:

Signal	Chip	Am9513 Counter	Source Pin	Gate Pin	Output Pin
0	1	1	1S1	1G1	1O1
1	1	2	1S2	1G2	1O2
2	1	3	1S3	1G3	1O3
3	1	4	1S4	1G4	1O4
4	1	5	1S5	1G5	1O5
5	2	1	2S1	2G1	2O1
6	2	2	2S2	2G2	2O2
7	2	3	2S3	2G3	2O3
8	2	4	2S4	2G4	2O4
9	2	5	2S5	2G5	2O5

Notes:

1. When choosing an internal gate or source it must reside on the same chip as output.
2. The output and counter are in one to one correspondence.
3. pulseCounter records implement 32 bit counters and thus use two am9513 counters. Two consecutive signals are used even though only one is specified. In addtion it is illegal to specify signals 4 or 9.
4. When a reference is made to GATE N, this means the same am9513 gate as the chosen am9513 counter. For example if Signal 7 is chosen, GATE N refers to 2G3.
5. SRCi refers to Am9513 source. If Signal is between 0 and 4 then SRCi refers to 1S1. If signal is between 5 and 9 then SRCi refers to 2Si. Similar conventions apply to GATEi
6. F1, ... F5 are internal clocks. F1 is a 4Mhz clock. The rate of each additional clock is the rate of the previous clock divided by 16. Thus the rates are:

   (F1,F2,F3,F4,F5) => (4MHz, 250 kHz, 15,625 Hz, 976.5625 Hz, 61.03515625 Hz)

   pulseDelay and pulseTrain devices always picks the optimum clock rate if an internal clock is chosen.