Timing System Performance

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Timing System of the SLS

Structure

−reference generation source, RF & AC line synchronization

−timing distribution (event system) −> "single" cable delivering all the machine timing to (practically) all the IOCs

Single source, fanout to multiple receivers

−operation sequencing & software using the event system facilities

Applications

−injection: Linac, pulsed magnets

−ramping of the Booster: magnets (fast internal ramp) &

RF (software ramp implemented in EPICS, 500 Hz clock)

−diagnostics: BPMs, synchronised cameras,

current transformers (ICT), tune measurement, etc.

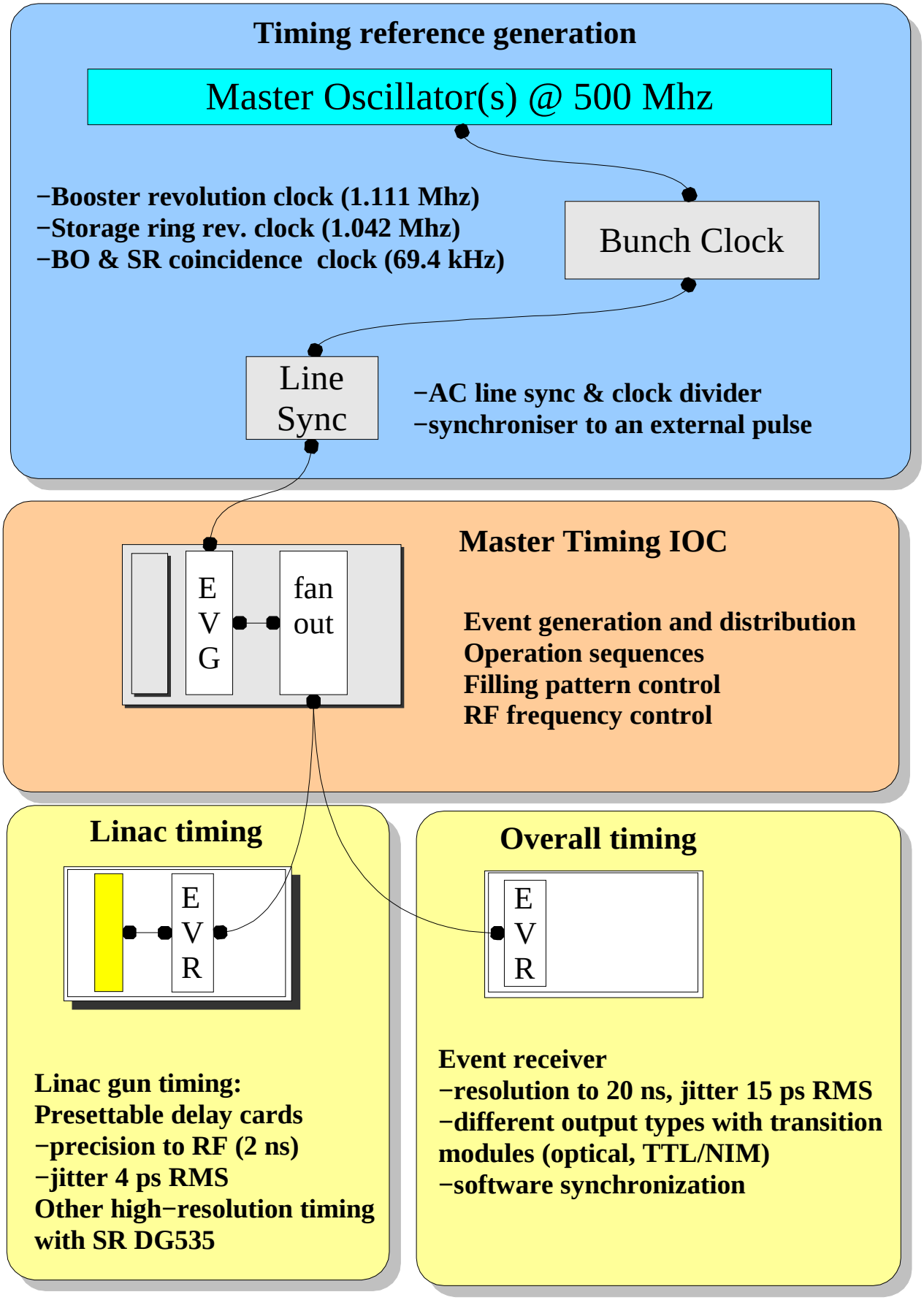
−synchronising over several IOCs

−fast beam dump (orbit−based, temperature based)

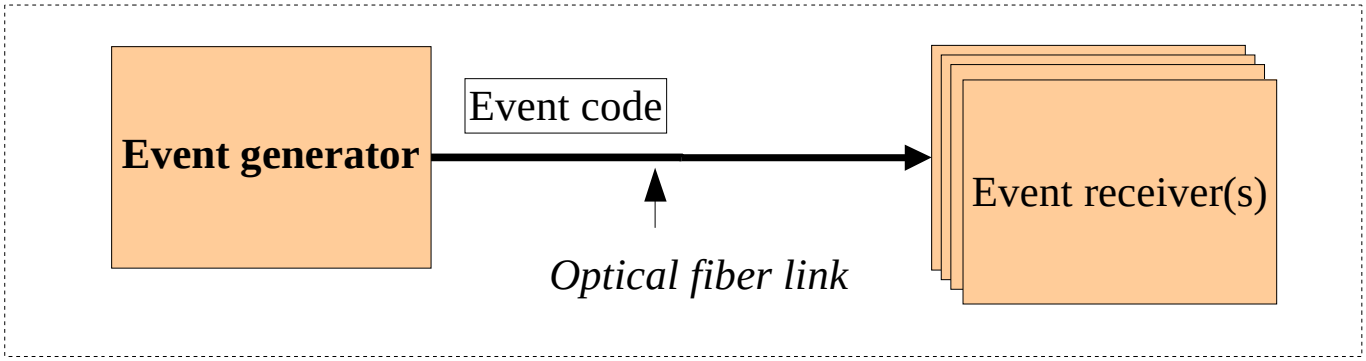
−high−precision, hardware assisted timestamps

−post−mortem machine state snapshot (future development)

Timing System Structure



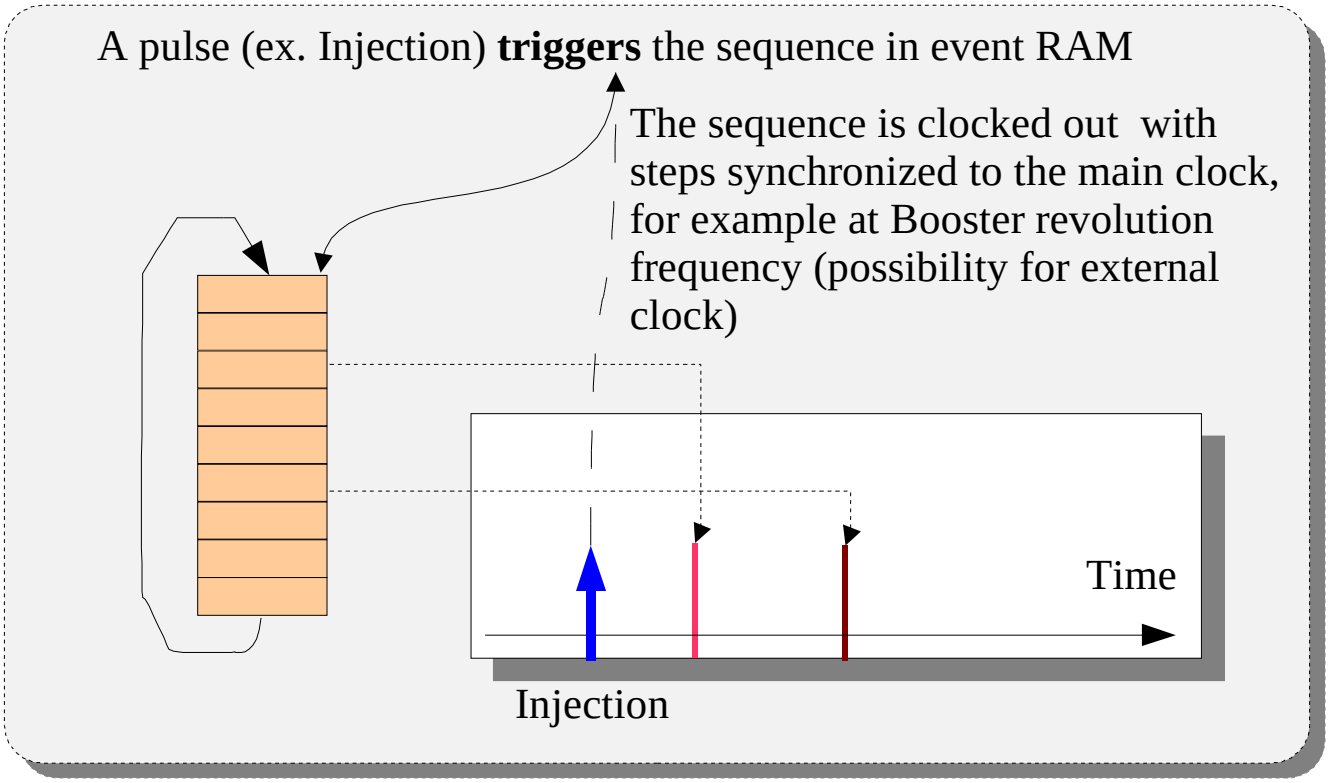
Event System Concept (APS)



Upon occurrence of an event,
an event code (8 bits) is transmitted over the optical fiber.
The **event** can be:
−**pulse on a hardware input**
−**software event** (write to a register)
−an entry in an **event RAM,that is clocked out** (cyclically).
This makes it possible to have programmed event sequences and easy modification with a software slider (for example).

Upon receival of an event code the receiver can:

−**output a pulse, immediately** or
−after a **delay**, with a specified **width**
−**process an EPICS record**
−**set or reset a signal** ("flip−flop")
Each event receiver can be programmed to respond in a different way to the same event code.



SLS Event system Features

Technology: Gigabit Ethernet, short wavelength (860 nm) fiberoptics transceivers (industry standard, several sources). Multimode (50/125 um) fiber

XILINX Virtex FPGA for the logic, loaded from flash ROM (in−system reprogrammable)
FPGA code written in VHDL

50 MEvents/second (50 MHz event rate), 20 ns resolution
Synchronized to the main RF oscillator

8−bit event codes plus 8 bits of individual bit transmission ("distributed bus")

Common PCB for generator and receiver

Downwards software compatible with the APS system.
Features added to support SLS extensions and operation

Fanout modules (VME): array of FO transmitters

−single line transmission of all timing information

−well integrated into EPICS (even to the regular record types) by APS

(SLS) Event Generator

3 possible event sources:
−hardware (TTL) inputs. 8 per card
−event generation by register write
−event RAMs for storing operator sequences (can also be used as a frequency generator!)

Several generators can be cascaded, for example to create a beamline−specific event circuit having all machine events

internal/external clock selection (we use clock derived from RF)

2 x 512 kEvent RAMs (external and internal clock, up to 8 MHz)
The system clock is derived from RF. By using the internal downconversion the RAM steps can be set to exact multiples of revolution period (for instance).

Alternate mode of RAMs: one RAM is active while the second is edited.

The SLS injector sequencing uses event RAMs with 0.9 us (500 MHz / 450) clock. (0.9 us = Booster revolution frequency)

prioritized event generation:

1. high−priority input (4)
2. RAM
3. low−priority input (4)
4. upstream EVG
5. SW generated event

SLS Event Receiver

Several types of outputs:
−4 programmable delay & width pulses:
up to 20 ns resolution, 16 bits (=1.3 ms) delay, width
Clock prescaler enables very long delays & widths with resolution tradeoff (from 20 ns to 1.3 m resolution and 1.3 ms to 8.6 sec local delays.)
−14 programmable width (20 ns−1.3 ms) output pulses
−7 set/reset "flip−flop" outputs

Trigger outputs phase locked to RF with a precision of 15 ps RMS.

Output signal type selected with use of the appropriate transition module. Transition modules used at SLS:
−opto: 14 optical outputs, for power supply ramp trigger
−NIM/TTL: NIM−level output, strong TTL to 50 ohm drive
−Straight−through: TTL

−VME interrupt facility for software synchronization
−delayed IRQ facility: hardware−delayed interrupt for fine−resolution software timing (e.g. Reading an ADC after 200 us)

−front panel RF−synchronised clocks (1, 5 and 100 MHz LVTTL)

−internal timestamp counter (in addition to clock events) enables very fine timestamp synchronization without using bandwidth for clock transmission. TS feature built into EPICS.

EPICS support for the event system

Record types to enable software control of

−mapping hardware input and output signals

−event generation from an EPICS record

−record processing upon receival of an event (timing signal)

−repetitive events and their placement in time (sequence RAM)

Event generator

EG record
−setup of the generator: mapping of hardware signals to events,RAM mode

EGEVENT record
−insertion of events into the event RAM.

Event receiver

ER record
−setup of the receiver: configuration of hardware signals (enable, delay generator setup, etc.)

EREVENT record
−event code to output mapping. Specifies what is the action upon receival of an event.

SLS−specific additions/modifications

−EG record: RAM prescaler & frequency fields
max delay (RAM position) field

−EGEVENT: priority handling of events (in RAM)

−ER record: pulse width fields for OTP, prescaler settings, IRQ delay settings, signal polarity selection

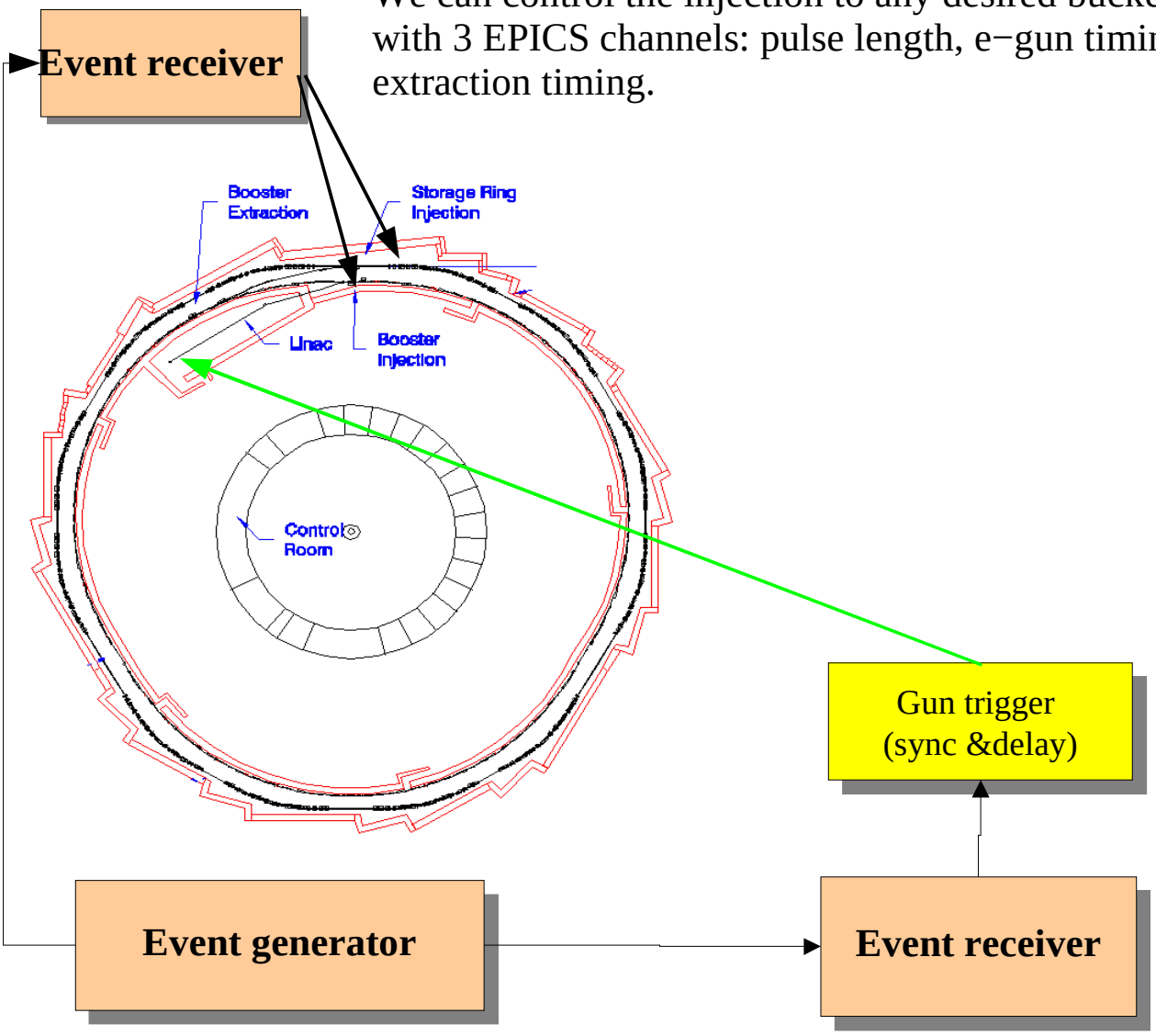
Injection timing control

The SLS Storage Ring has **480** RF buckets, the Booster has **450**. At the coincidence of SR period and Booster period pulses (superperiod) the rings have their #0 bucket in alignment. From that instant the buckets proceed as

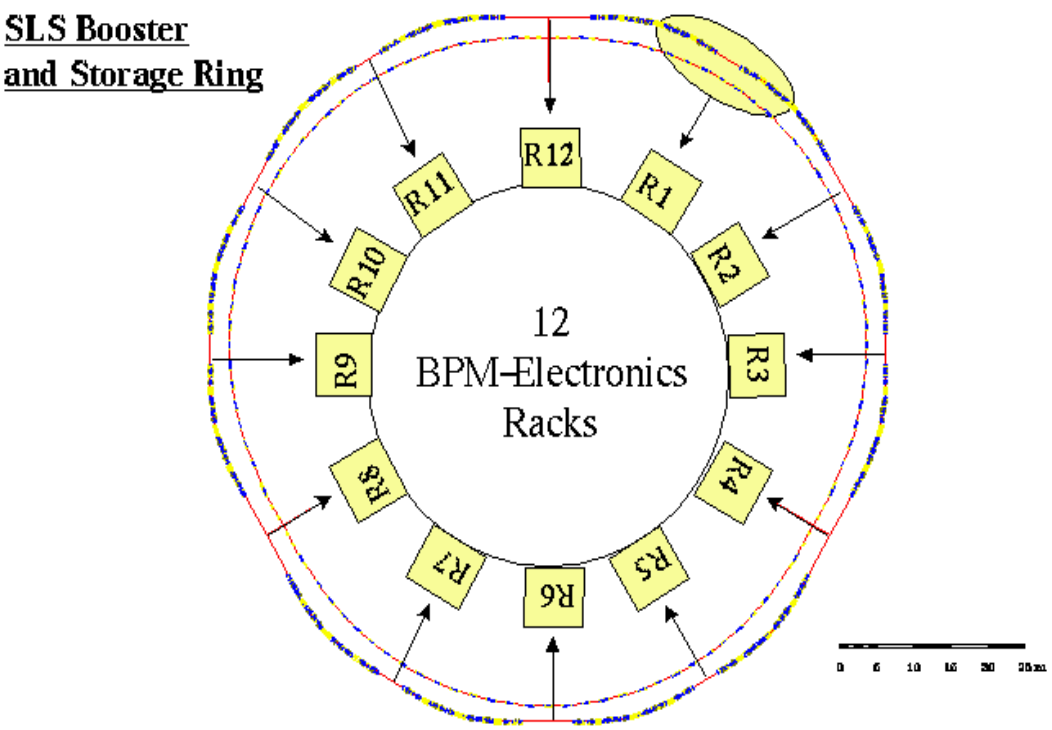
```
BO  000 001 002 003 ... 449 000 001 ... 028 029 030 031 ...
SR  000 001 002 003 ... 449 450 451 ... 478 479 000 001 ...
```

and so on. The #0 buckets will be in alignment every 16th Booster period. The time of extraction is defined by setting a timing event in the correct position in the event generator RAM. By moving that event one position (one Booster turn), the injection to SR is shifted by 30 buckets. Finer level adjustment is done in the linac (e−gun trigger)

We can control the injection to any desired bucket with 3 EPICS channels: pulse length, e−gun timing, extraction timing.



Timing & Control for BPM system



Per BPM crate 1 event receiver.

The BPMs (in turn−by−turn mode) need a synchronizing trigger to start acquisition. This is delivered through the event system. The same event also triggers the chain of EPICS records to process the data.

The BPM sync event follows the SR injection timing with an offset that the operators can set. The following feature can be disabled.

For individual stations: 1 turn in SR = 960 ns; with exact spacing, the delay between BPM stations = 80 ns.

Comments

−Existing EPICS support was a big advantage:
    We had the basic functionality and could incrementally
    add the features that we needed

−Hardware has proven to be very reliable

−Number of applications is large and growing
    (timing ioc debug time is scarce...)

−very few timing (system) problems during operation

EPICS problems:

−Timestamp support needs some improvements (work in progress)
    master timing IOC resynchronisation
    defaulting to event slave even when EVR is not in operation
    non−integer clock rates
−EVG alternate RAM operation
    cause for occasional loss of events due to RAM updates
    by asynchronous clients?