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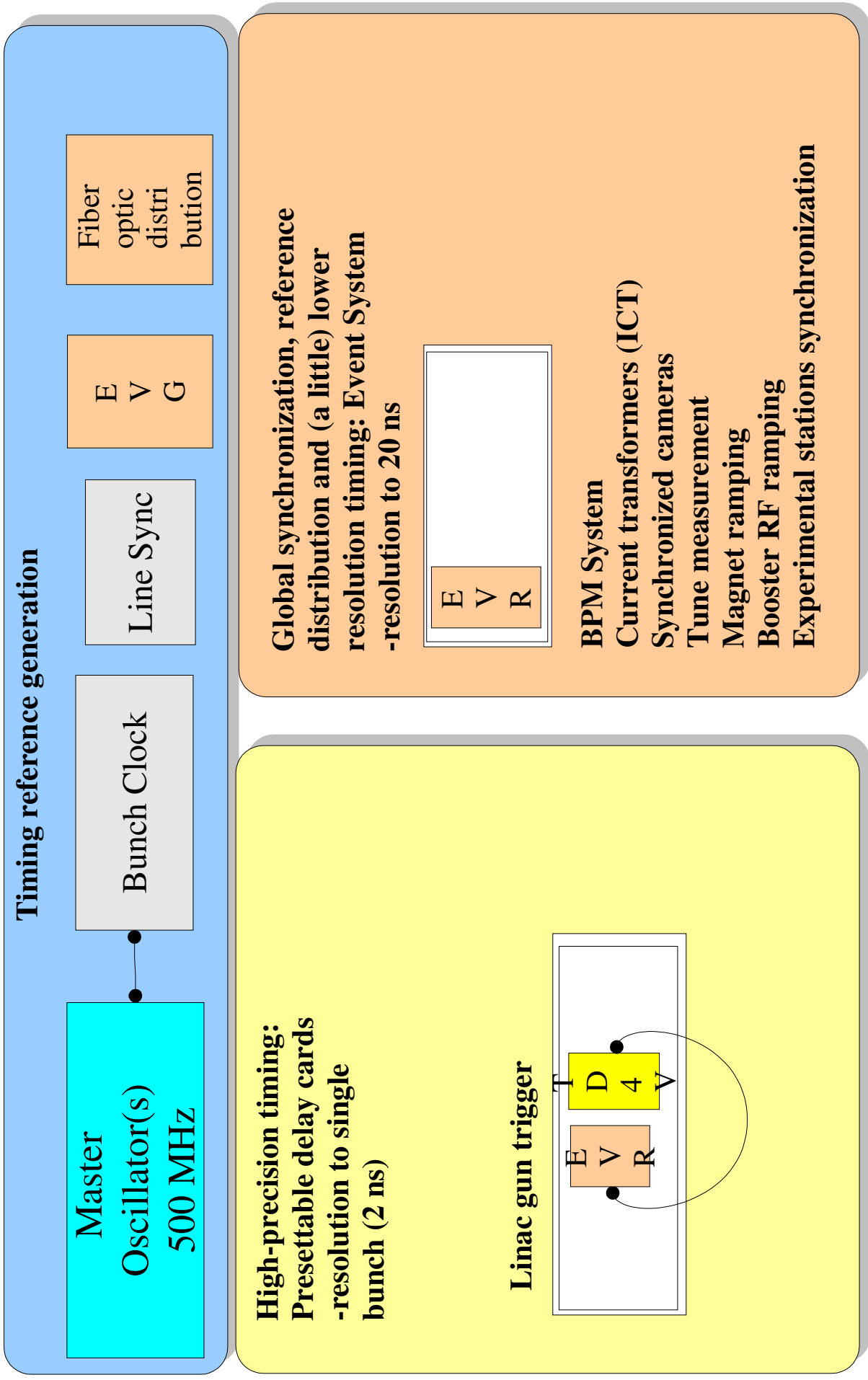
# Timing Pattern Generator of the Swiss Light Source

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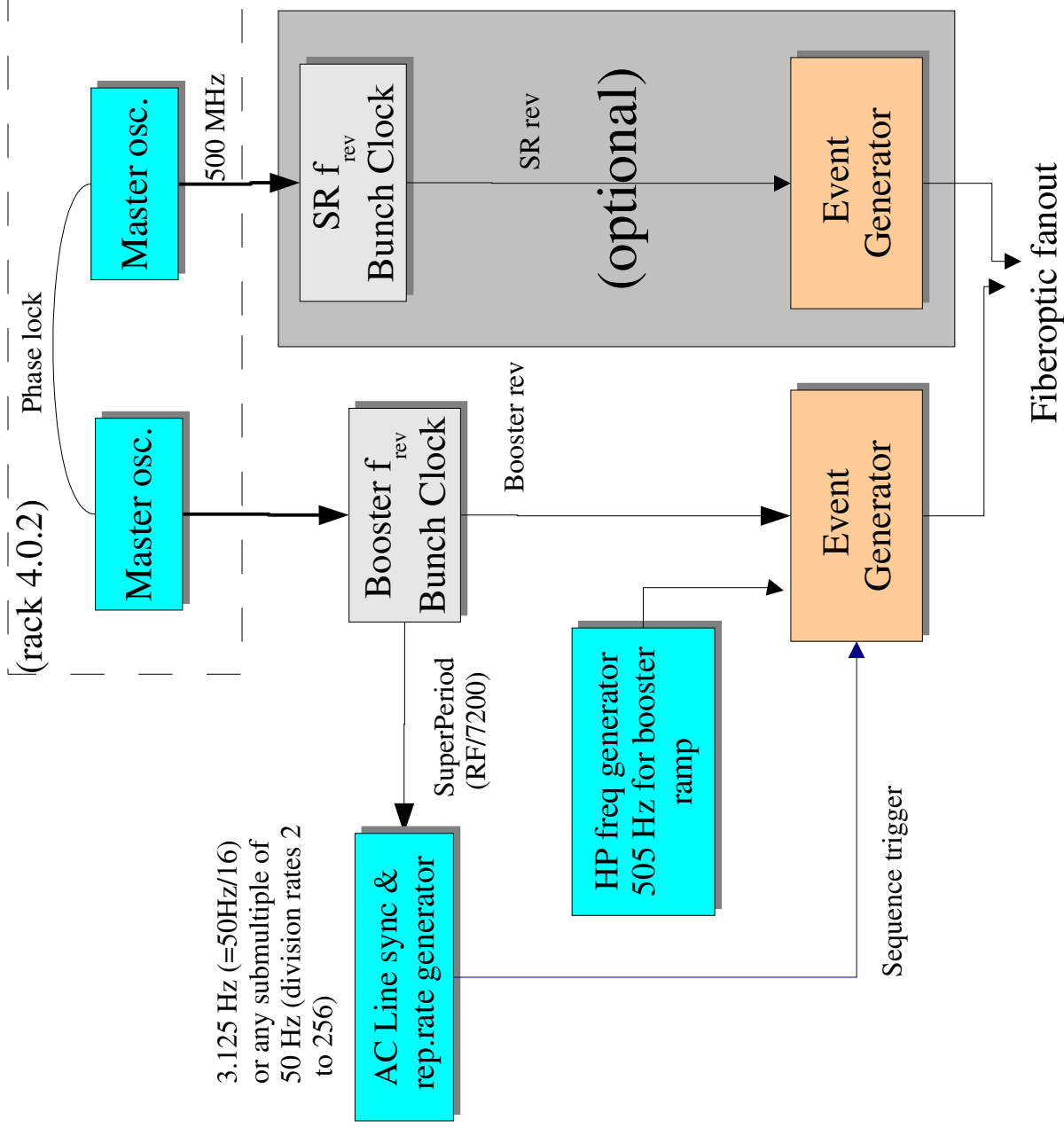
- present setup
- new developments
- EPICS support
- applications



# Timing System Structure



# Current SLS Timing Source



Most operations already built into event system. However, some homegrown or external components remain:

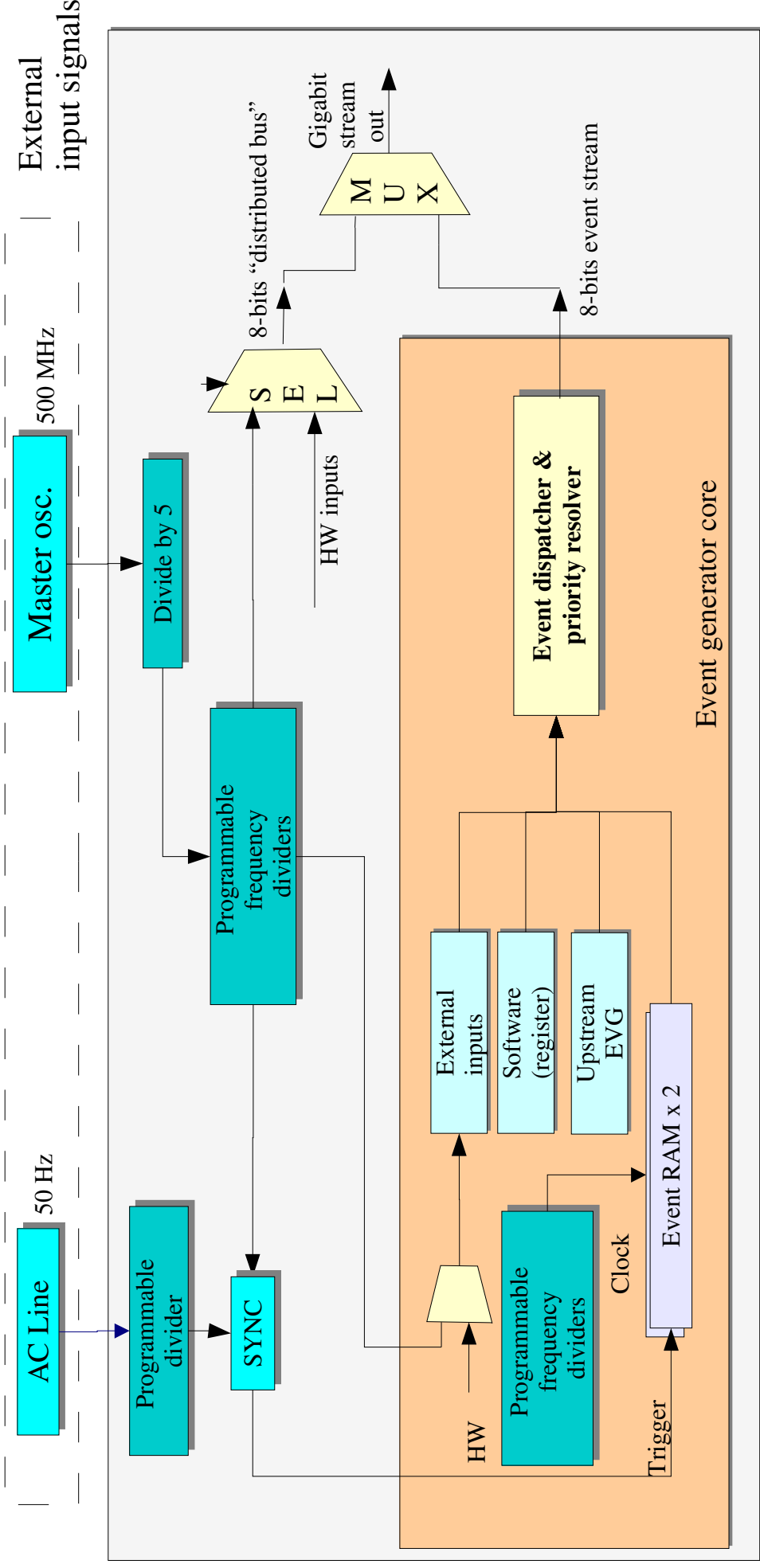
- AC line sync
- Bunch clock
- External clock generator (HP)

User's need for more clocks with settable frequencies led to an idea: **build all these directly into EVG.**

Advantages:

- eliminate external 'boxes'
- simplify software
- better performance
- simplify maintenance

# Timing Source with EVG-Plus



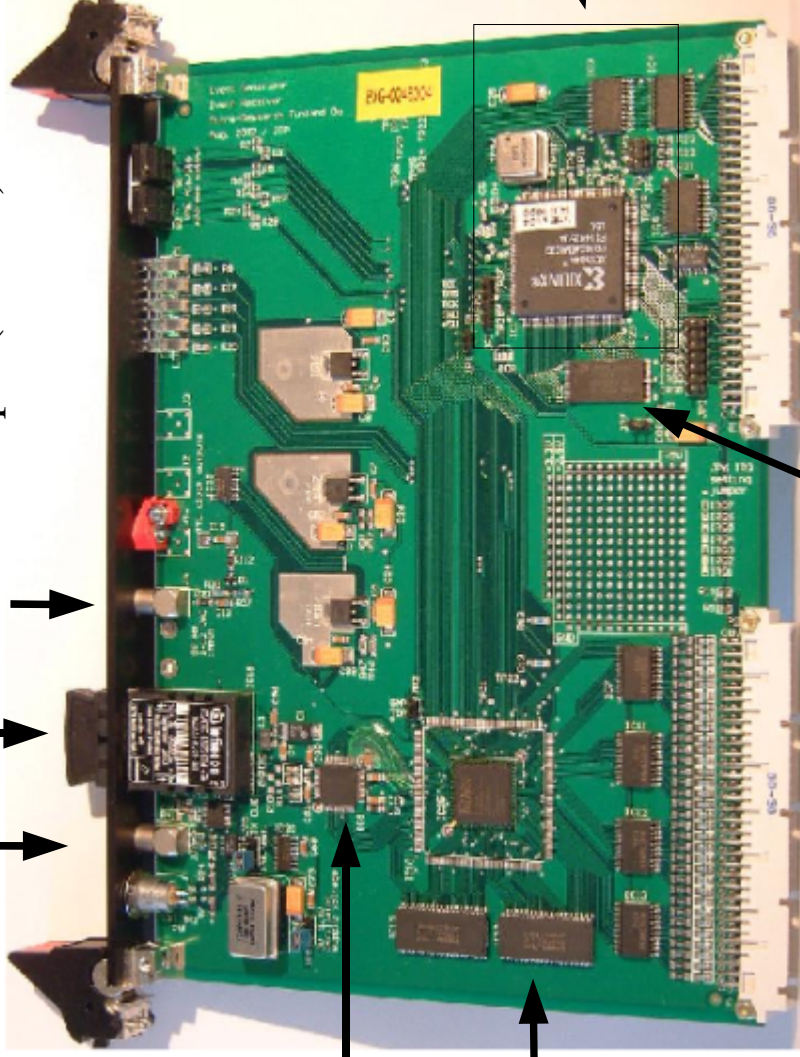
“Timing system on one card” : only AC and RF signal inputs needed. Everything else is under software control.

## EVG Plus Card

RF (500 MHz) input

Fiberoptic Transceiver

AC line input (3-12 V)



Gigabit Ethernet  
Transceiver chip  
(ser/par conversion,  
framing, PLL, etc.)

Event RAMs  
(2 x 512kB)

VME interface

Flash memory for FPGA configurations



## EPICS support for the Event Generator

Record types for supporting EVG (original APS, SLS extensions)

**EG** record, setup of the generator:

- mapping of hardware signals to events
- enable/disable of HW inputs
- RAM mode
- RAM clock prescaler setting
- RAM software triggers
- Software event generation (VME)

New features (to be done):

- prescaler frequency settings (for 8 new)
- AC line prescaler
- selection of distributed bus input (external in/prescaler)
- prescaler to event trigger selection
- prescaler&AC sync to RAM sequence trigger selection

**EGEVENT** record, placement of events into the event RAM.

- event number
- delay (desired & actual)
- delay unit
- RAM #
- priority
- max. delay

On the wishlist:

- a better (simpler, more efficient) way to handle alternate RAM updates. Works, but is complicated and unnecessarily slow.

## New Applications

Driving requirement:  
generation of clock signals for time-resolved experiments:  
revolution clock (1 pulse/storage ring turn) and subharmonics  
(available now, although with limited EPICS support)

Additional need for high-precision timing at the beamline  
development for an event receiver with 500 MHz regeneration in progress

Experiment start planned for summer 2003

Flexible, jitter-free clock signals for beam diagnostic purposes (not always possible with events)