Running an embedded EPICS IOC over µClinux on the Nios II soft core processor

Doug Curry and Alicia Hofler

Jefferson Lab

Overview

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- FPGAs
- Soft Core Processors
- μClinux
- Cross-Compiling EPICS
- Running an EPICS IOC on Custom Hardware
- Summary

Motivation

- Embedded IOCs expand portability/flexibility
  - Operating environment is no longer part of the design constraints (VME/Serial)
    - Reduce multiple long cable installations
    - Single communication cable
  - Chassis or other working environment can house the IOC
- Multiple small "specialized" IOCs
  - Decrease system coupling
  - Increase individual system availability
- Soft Core Processors integrate easily with the custom logic, eliminate master/slave approach

FPGAs

- Low cost
- Large component counts
  - Modern FPGA families are built on 130 nm and 90 nm processes
- Typical digital design implementations and simulations are done using VHDL or Verilog
- Highly configurable platforms (SRAM based devices)
  - Tolerant to design changes throughout the development process and even well after design completion
- Error Detection
  - CRC checks of configuration memory (built into the device)
  - State machine fault detection (implemented with design code)

Soft Core Processors

- Flexible Processor Architecture
  - Single stage execution, up to 6 stage pipeline
  - User defined instruction/data cache sizes, flexible ALU, DMA controller, dynamic branch prediction
- Fixed Instruction Set Architecture
- Fits into any modern FPGA family
- Processor core is programmed directly into the FPGA fabric
- Eliminate master/slave bottleneck of typical system platforms
- Processor core is generated in VHDL or Verilog
  - Single core ports to multiple designs
  - System identification number is generated at design time
    - Use for configuration control (162, 167, 177, PPC, etc…)

µClinux

- Linux is a supported EPICS platform
  - Cross compiling is therefore somewhat less complicated
- µClinux is a port of Linux for systems lacking Memory Management Units
  - Current Nios II architecture does not have an MMU
- Nios II port is already done (preliminary)
- Altera hopes to have their MMU completed within the next year
  - Red Hat Linux support

Cross Compiling EPICS

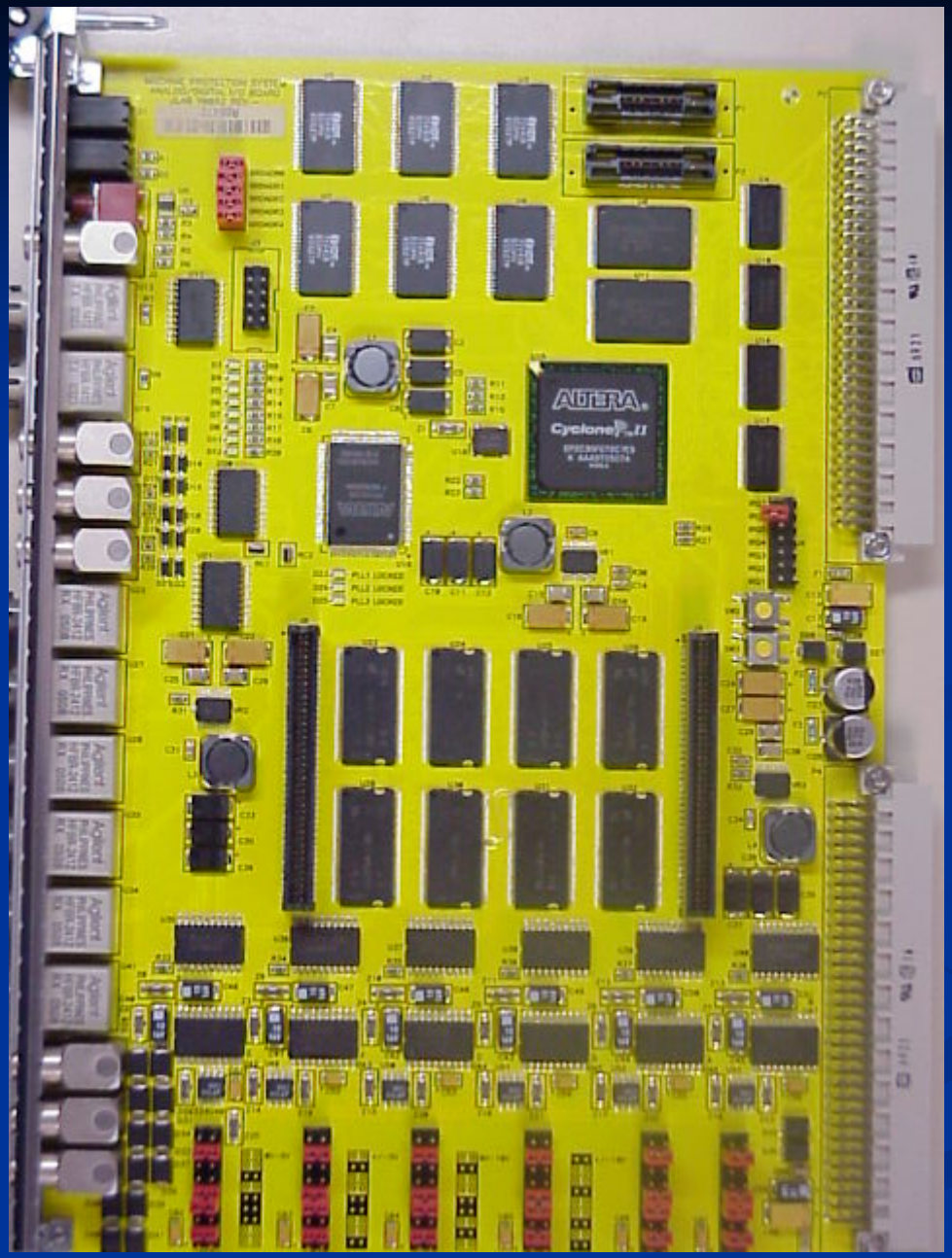
- Standard cygwin installation is required for Windows host builds
- Current compilation for μClinux targeting the Nios II ISA has been completed using the cygwin environment
- IOC does not initialize correctly
  - Startup file (crt0.o) does not call global CTORs
- Explicit call to iocshRegisterCommon() is required in order to get minor functionality
  - dbLoadDatabase("some.dbd")

Running an Embedded IOC on Custom Hardware

- Embedded IOC for $100
- Additional components required
  - Flash (kernel, file system)
  - SDRAM or DDRAM
  - Ethernet Controller Hardware
- EPICS files stored on a NFS server
- Embedded processor and digital logic co-exist in the same FPGA
  - Operate independently
  - Processor uses space that is already available

Summary of Embedded IOCs

- Increase design flexibility and decrease system coupling
- Embedded IOCs running over the FPGA fabric are fairly inexpensive and are easier to integrate with the existing digital design
- Linux is already a supported EPICS platform; however, μClinux requires additional configuration
- Details of global CTORs/DTORs not being called by the startup file need to be worked out



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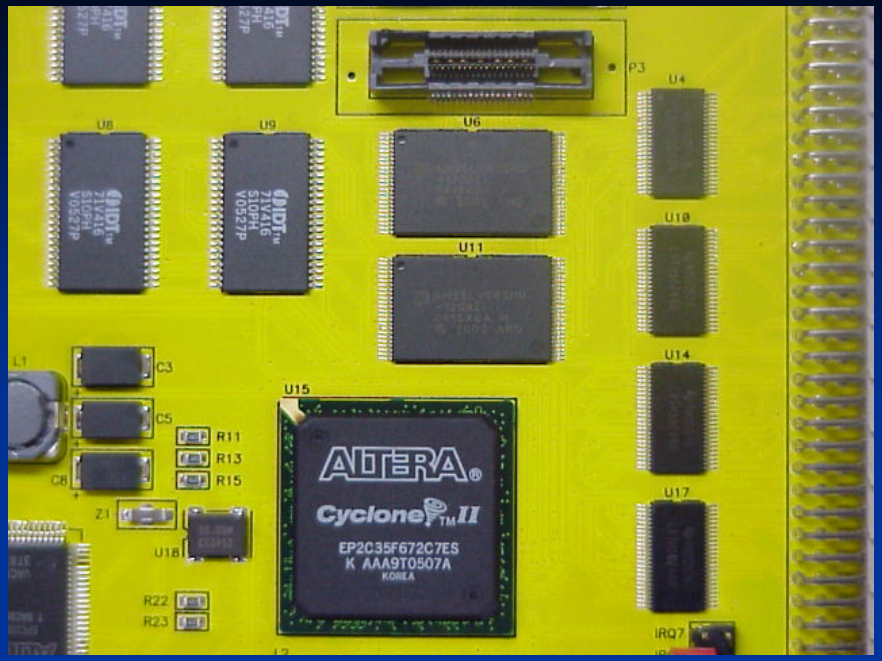
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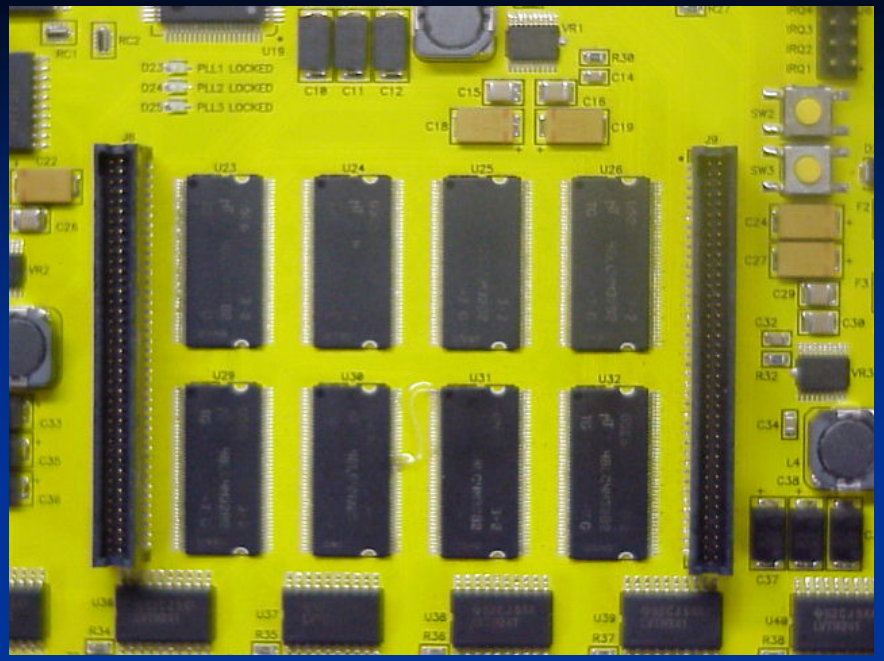

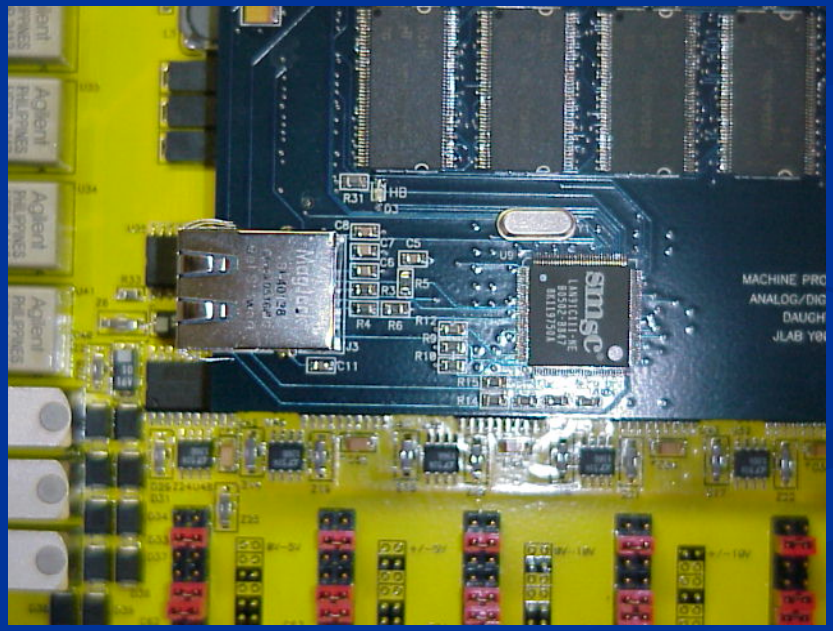
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