



Embedded IOC Applications at the APS

2005-10-06

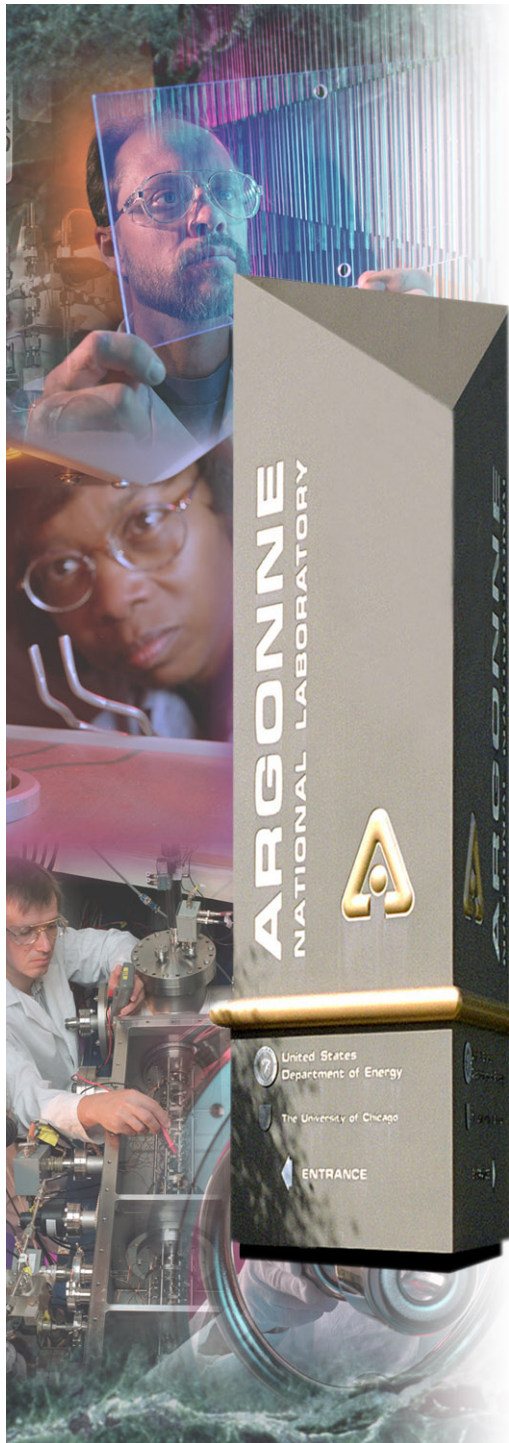
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Arcturus uCDIMM ColdFire 5282 module



- Motorola/FreeScale ColdFire 5282 processor (64 MHz)
- 16 Megabyte SDRAM (32-bit data path)
- 4 Megabyte flash memory (RTEMS/EPICS/IOC)
- 1/2 Megabyte on-chip flash (bootstrap)
- SO-DIMM form factor
- ~\$200 in small quantities, \$120 each for orders of 500 or more.

Arcturus uCDIMM ColdFire 5282 module



- 10/100 Mb/s Ethernet (10/100 BaseT)
- 3 serial ports (2 RS-232, 1 LVTTL)
- I²C and SPI
- CAN support
- 8-channel, 10-bit ADC
- A24/D16 external bus
- 5 interrupt request lines
- 16 general-purpose I/O lines

EPICS device support

- **Ethernet and serial ASYN drivers**
- **I²C ASYN driver**
 - Tested with MAX1619 temperature monitor
 - Easy to add support for additional devices (GPIB-style)
- **QADC device support for analog-in record**
 - Scanning (“voltmeter”) operation
- **Watchdog timer device support for binary-out record**
 - Hardware reset on failure to process record in 5 second interval
- **Flash memory programming device support**
 - Remote updates of application using standard EPICS tools
- **devLib support**
 - ‘VME’ devices implemented in Altera FPGA (Avalon)

□ Altera Avalon Bus

- **Altera “System on a programmable chip” technology**
- **Appears to designer as multiple master/slave bus**
- **Masters can be active simultaneously (to different slaves)**
- **Example Master devices**
 - NIOS processor (on-chip)
 - ColdFire bridge
- **Example Slave devices**
 - On-chip memory
 - Off-chip SDRAM
 - Parallel I/O port
 - Application-specific

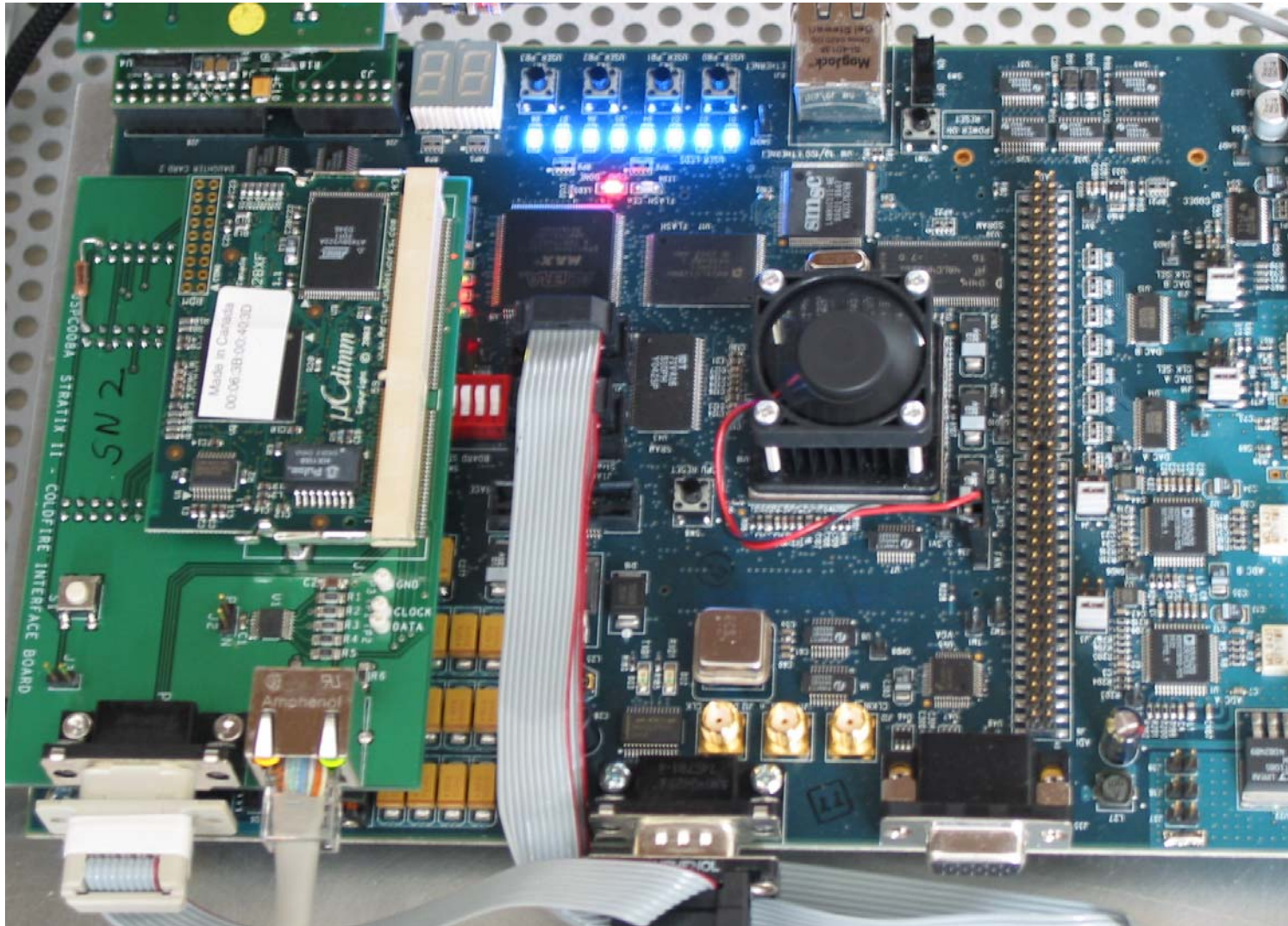
uCDIMM ColdFire 5282 Bridge

- **Separate ColdFire/Avalon clock domains**
- **25-bit Avalon address space (16-bit data bus to ColdFire)**
 - ColdFire sees
 - *Full VME A24/D16*
 - *Full VME A16/D16*
 - *Subset of VME A32/D32*
- **Full Avalon interrupt support**
 - Avalon interrupts 0 to 63 map to VME interrupts 192 to 255
- **ColdFire IOCs can use standard devLib VME support**
- **Very low resource usage (49 ALUTs, 31 registers)**
 - Less than 0.1% of the chip used for several APS applications

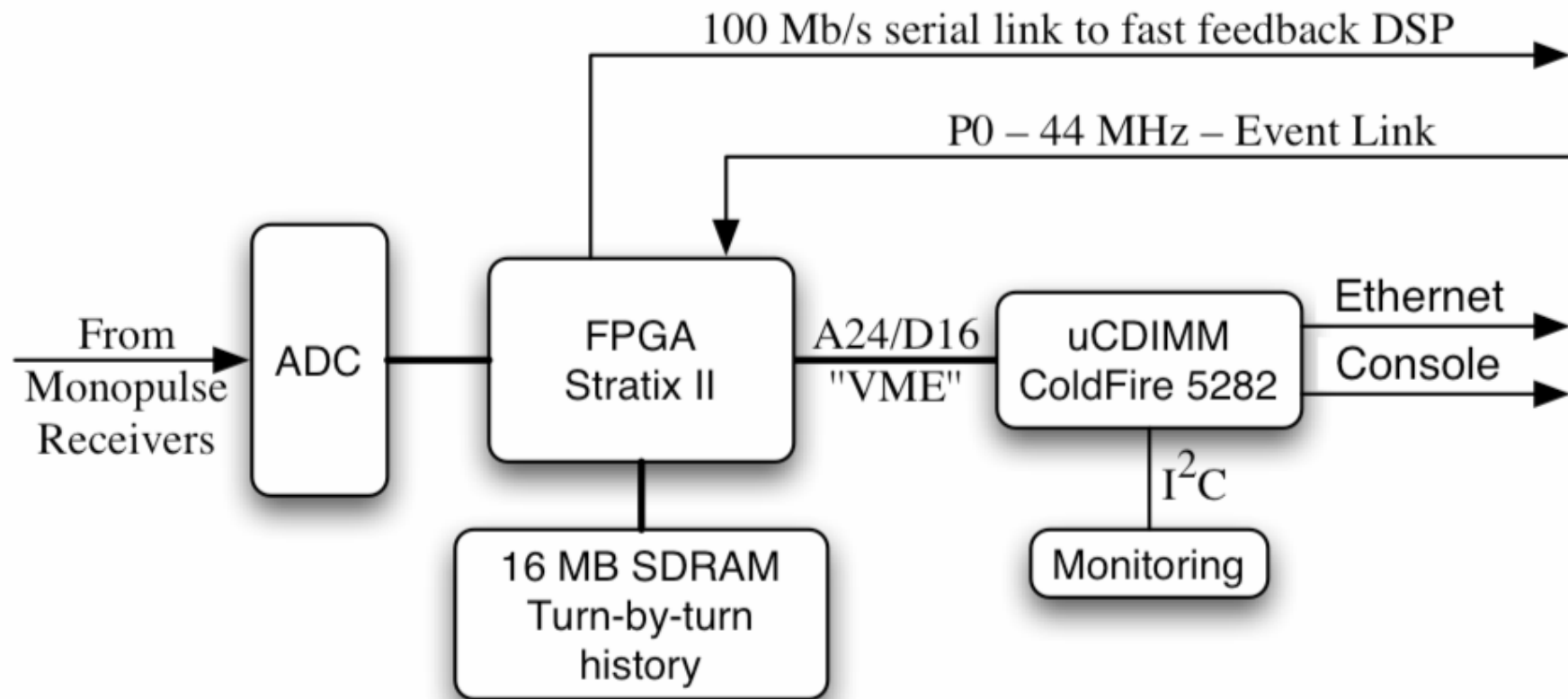
uCDIMM – Altera Transition Card

- **SO-DIMM connector for uCDIMM ColdFire 5282 card**
- **Console (DB-9) and Ethernet (RJ-45) connectors**
- **DS1619 digital thermometer chip**
 - Ambient temperature
 - FPGA core temperature
- **Connects to development kit ‘expansion prototype’ connectors**
- **Tested with several Altera development kits**
 - Stratix II DSP
 - Stratix II NIOS
 - Cyclone II NIOS

uCDIMM mounted on Stratix II DSP kit



uCDIMM application – SR BPM Prototype



SR BPM Prototype – SOPC Builder

Use	Module Name	Description	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>	<input type="checkbox"/> coldfirebridge_0	ColdFireBridge	clk			
	ColdFireMaster	Master port				
<input checked="" type="checkbox"/>	<input type="checkbox"/> apseventreceiver_0	APSeventReceiver	clk			
	APSeventReceiver	Slave port		0x01FF8800	0x01FF887F	2
<input checked="" type="checkbox"/>	<input type="checkbox"/> filters_0	Filters	clk			
	Filters	Slave port		0x01014000	0x010143FF	
<input checked="" type="checkbox"/>	<input type="checkbox"/> prototwoadc_0	ProtoTwoADC	clk			
	ScopeControl	Slave port		0x01014400	0x0101441F	0
	ScopeRam	Slave port		0x01000000	0x0100FFFF	
	AdcControlRam	Slave port		0x01010000	0x01013FFF	
<input checked="" type="checkbox"/>	<input type="checkbox"/> turnhistory_0	TurnHistory	clk			
	TurnHistoryControl	Slave port		0x010144A0	0x010144BF	1
	TurnHistoryFillMaster	Master port				
<input checked="" type="checkbox"/>	<input type="checkbox"/> sdram_0	SDRAM Controller	clk			
	s1	Slave port		0x00000000	0x00FFFFFF	
<input checked="" type="checkbox"/>	<input type="checkbox"/> indirectmaster_0	IndirectMaster	clk			
	IndirectSlave	Slave port		0x01FFFC0	0x01FFFCF	
	IndirectMaster	Master port				
<input checked="" type="checkbox"/>	<input type="checkbox"/> tri_state_bridge_0	Avalon Tri-State Bridge	clk			
	avalon_slave	Slave port				
	tristate_master	Master port				
<input checked="" type="checkbox"/>	<input type="checkbox"/> cfi_flash_0	Flash Memory (Common Flash Interface)		0x00000000	0x00FFFFFF	

SR BPM FPGA EPICS device support

- **Avalon APS event receiver**
 - EPICS driver identical to vxWorks/VME version
- **ASYN 'int32' and 'float64' drivers**
 - Acquisition-control waveform record
 - Filter coefficients
 - Clock status
 - PLL reconfigure (programmable delay, 160 ps steps)
- **Generic Transient Recorder drivers**
 - 'Digital Oscilloscope' display of raw ADC values (4096 points)
 - Turn history (262144 points)

Single-bunch feedback

- **Transverse beam stabilization**
- **Each 88 MHz clock interval (11.26 ns):**
 - Sample horizontal BPM ADC (12-bit)
 - Update/remove DC offset
 - Apply 32-tap FIR filter (18-bit coefficients, 18-bit values)
 - Apply per-bunch gain
 - Programmable delay
 - Drive DAC (14-bit)
- **$\sim 3 \times 10^9$ multiply-accumulate operations/second**
- **EPICS drivers for:**
 - Filter coefficients, bunch gains
 - Clock status
 - Programmable delay

Smart power supply controller

- **Under development**
- **Replace Power Supply Control Units and BITBUS interface**
 - Eliminate obsolescence issues with some components
 - Provide additional capability.
- **Will add ~220 IOCs to control system**
 - Network segmentation (routers)
 - EPICS channel access segmentation (gateways)
 - Second tier network switches (one per double-sector)
 - Additional terminal servers for console ports

Smart power supply controller

