Timing Sytem Developments

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Micro-Research Finland Oy

- Founded in 1985
- VME data transfer products in late 80's early 90's (e.g. VMExi2)
- Timing System development initiated in 1999 by the design of the timing system for SLS (series 100)
- References:
  - SLS, Paul-Scherrer Institute, Switzerland
  - Diamond Light Source Ltd., U.K.
  - ASP, Australia
  - BEPCII, Insitute for High Energy Physics, Beijing, China
  - LCLS, Stanford Linear Accelerator Center, USA
  - SNS, Oak Ridge National Laboratory, USA
  - SSRF, Shanghai, China
  - Elettra, Trieste, Italy
  - And others...

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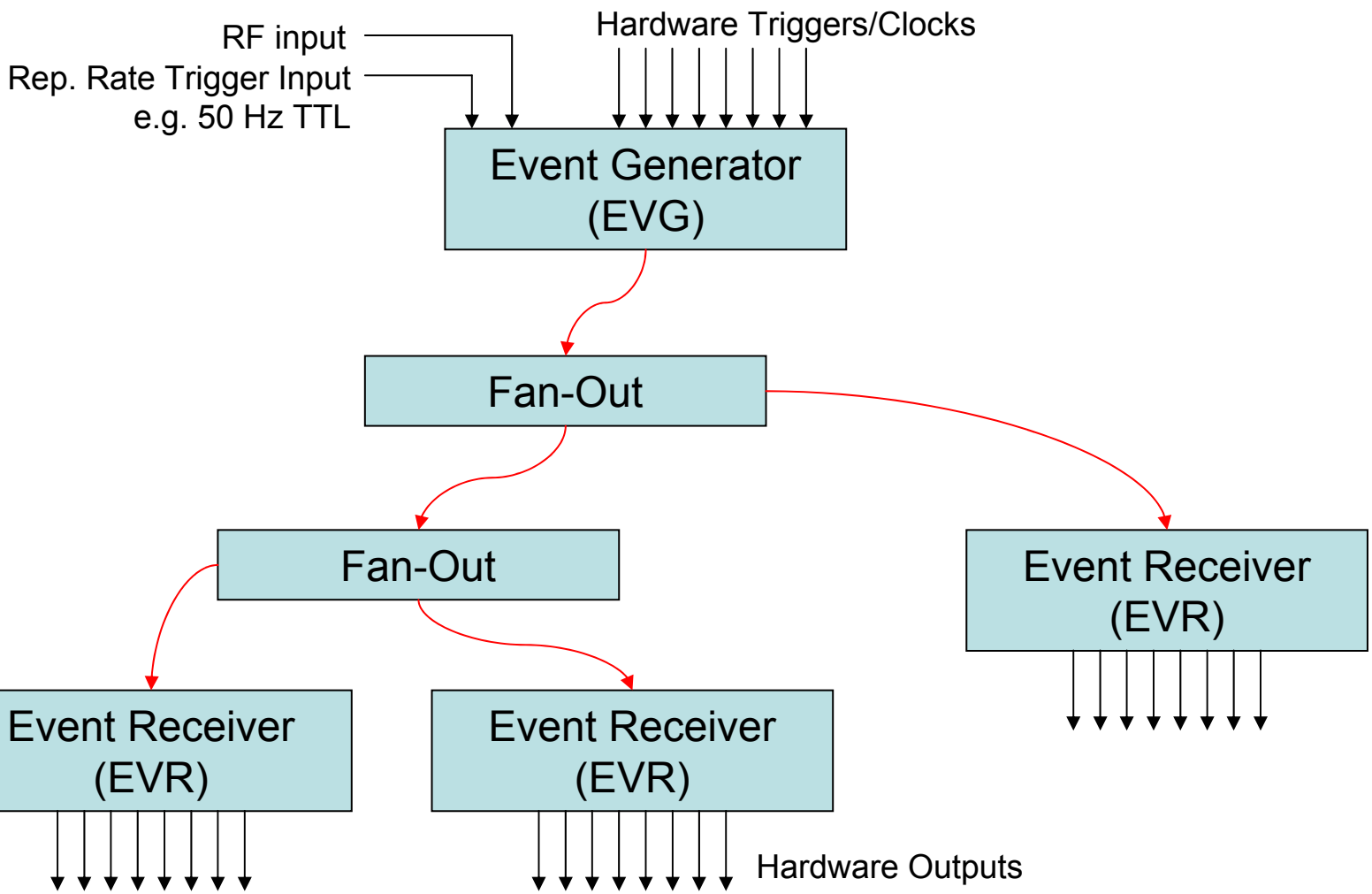
Timing System Overview



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Timing System Principles

- Event driven system, 255 event codes
- Events are sent out with the event clock rate which is derived from the RF reference
- Eight distributed bus signals, updated simultaneously at the event clock rate
- Multiple sources for events: e.g. External, Sequencer, software
- Multiplexed counters can be used to generate fiducials, e.g. SR, booster clock, COIC for synchrotrons
- Event Receivers generate pulse outputs with programmable delay and width
- Support for Timestamping/distribution of time
- Data transfer support with predictable timing

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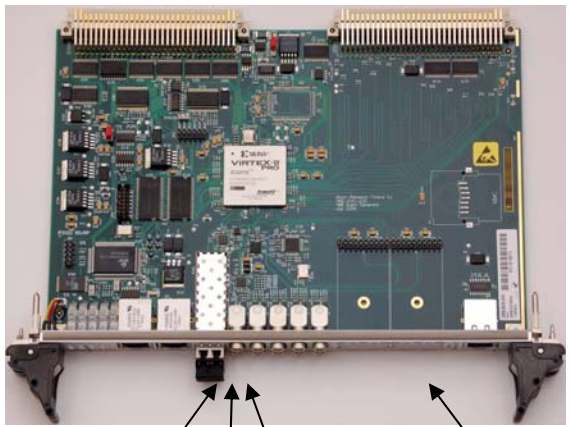
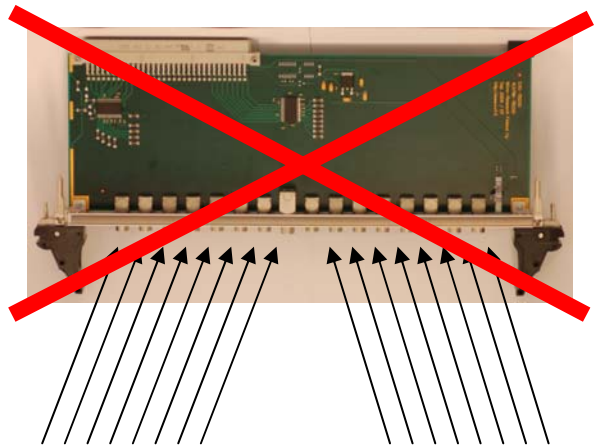
Event Generator (VME-EVG-230)





Distributed bus inputs

External trigger inputs

Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

SFP transceiver
• Optical signal to EVRs (fan-outs)

RF input
• Event clock divided from RF /1, /2, ... , /32
• Event clock 50 – 125 MHz

Line syncronisation input
e.g. 50 Hz / 60 Hz TTL level

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Event Generator (cPCI-EVG-220)

Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

Line syncronisation input
e.g. 50 Hz / 60 Hz TTL level

RF input
• Event clock divided from RF
• /1, /2, ... , /32
• Event clock 50 to 100 MHz

SFP transceiver
• Optical signal to EVRs (fan-outs)

Optional side-by-side I/O extension module for three Universal I/O slots, providing up to six I/O signals

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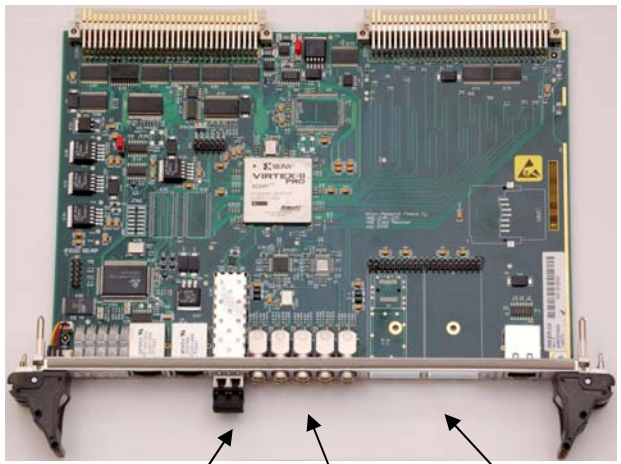
VME Event Receiver (VME-EVR-230)



HTB OTB TTB NTB

SFP transceiver
• Optical signal from EVG (or fan-out)

Programmable outputs
• 8 TTL level
• External trigger input

Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

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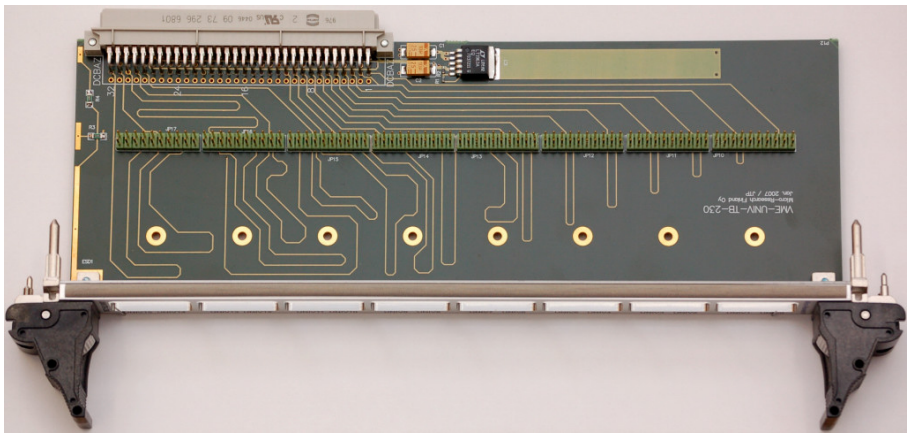
VME Universal I/O Transition Board (VME-UNIV-TB)



- Carries up to eigth Univesal I/O Modules
- Same Transition board for both EVG and EVR

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Universal I/O Modules

- 25.4 mm x 52 plug-in units
- two outputs or inputs each
- can be fitted on VME-EVG-230 and VME-EVR-230(RF), VME-UNIV-TB, CompactPCI EVG/EVR, CompactPCI side-by-side module

Optical HFBR-1414

820 nm

Optical HFBR-1528

650 nm
1 mm POF

NIM Output

TTL Output

TTL Input

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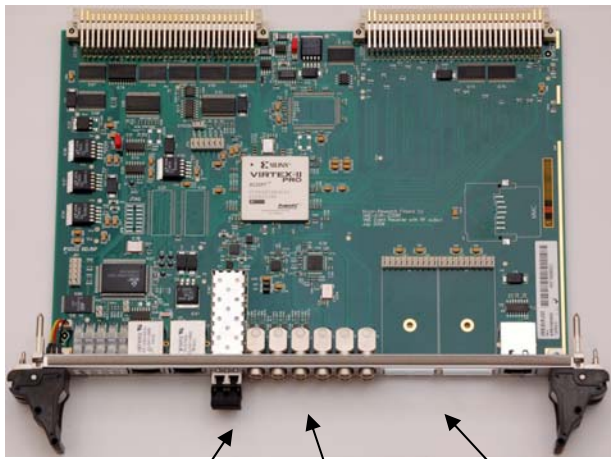
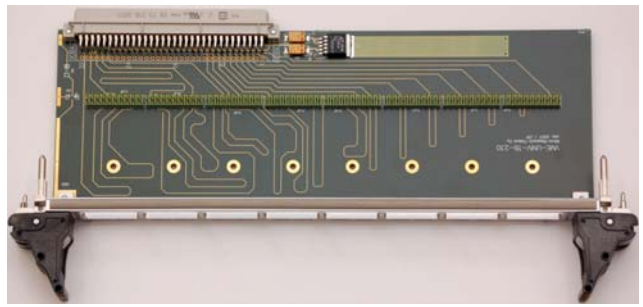
VME Event Receiver with RF output (VME-EVR-230RF)





Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

SFP transceiver
• Optical signal from EVG (or fan-out)

Programmable outputs
• 4 TTL level
• External trigger input
• External inhibit input

• 3 Differential CML RF/pattern outputs with 1/20th event cycle resolution (400 ps @ 8 ns event clock cycle)

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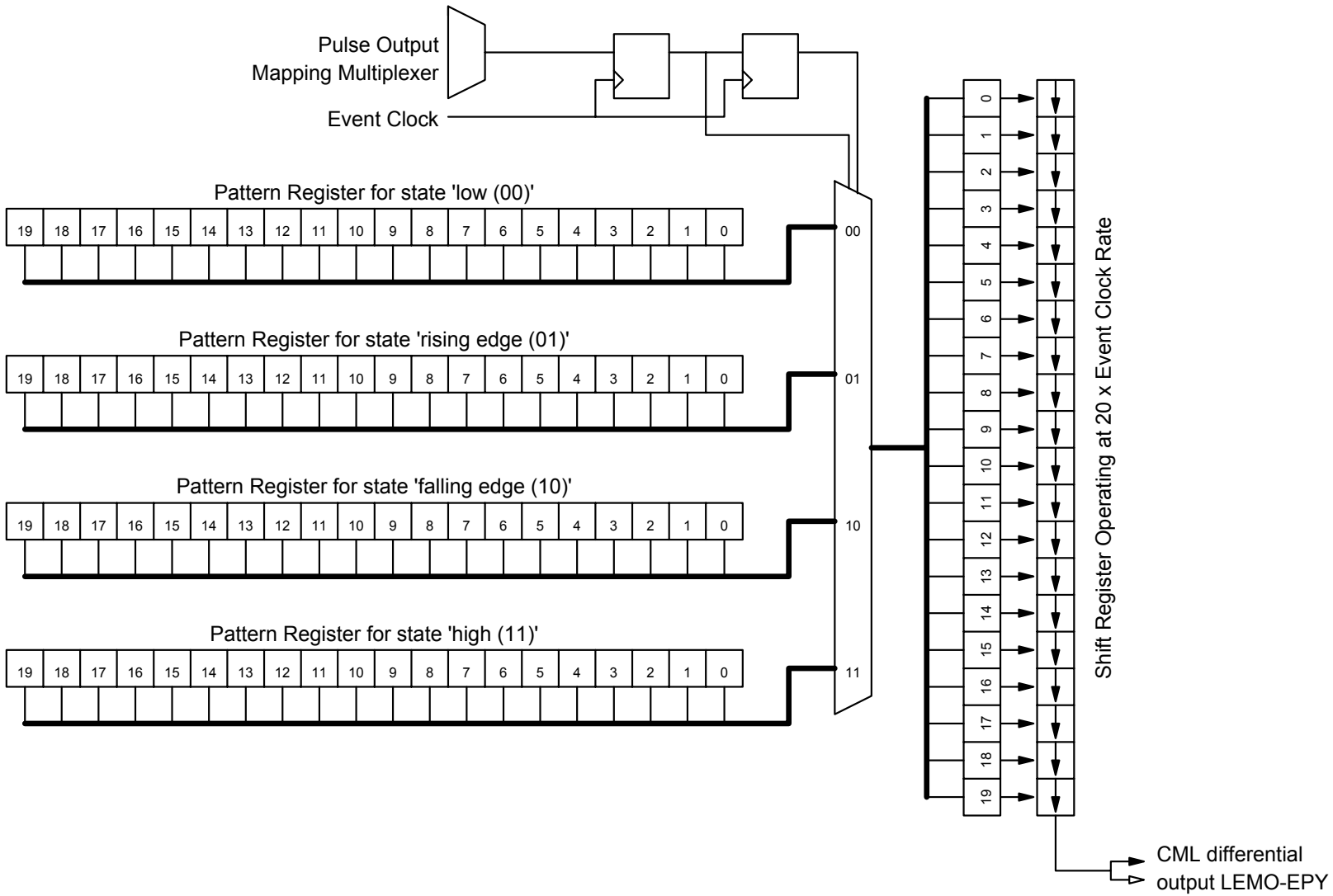
CML pattern outputs (VME-EVR-230RF)



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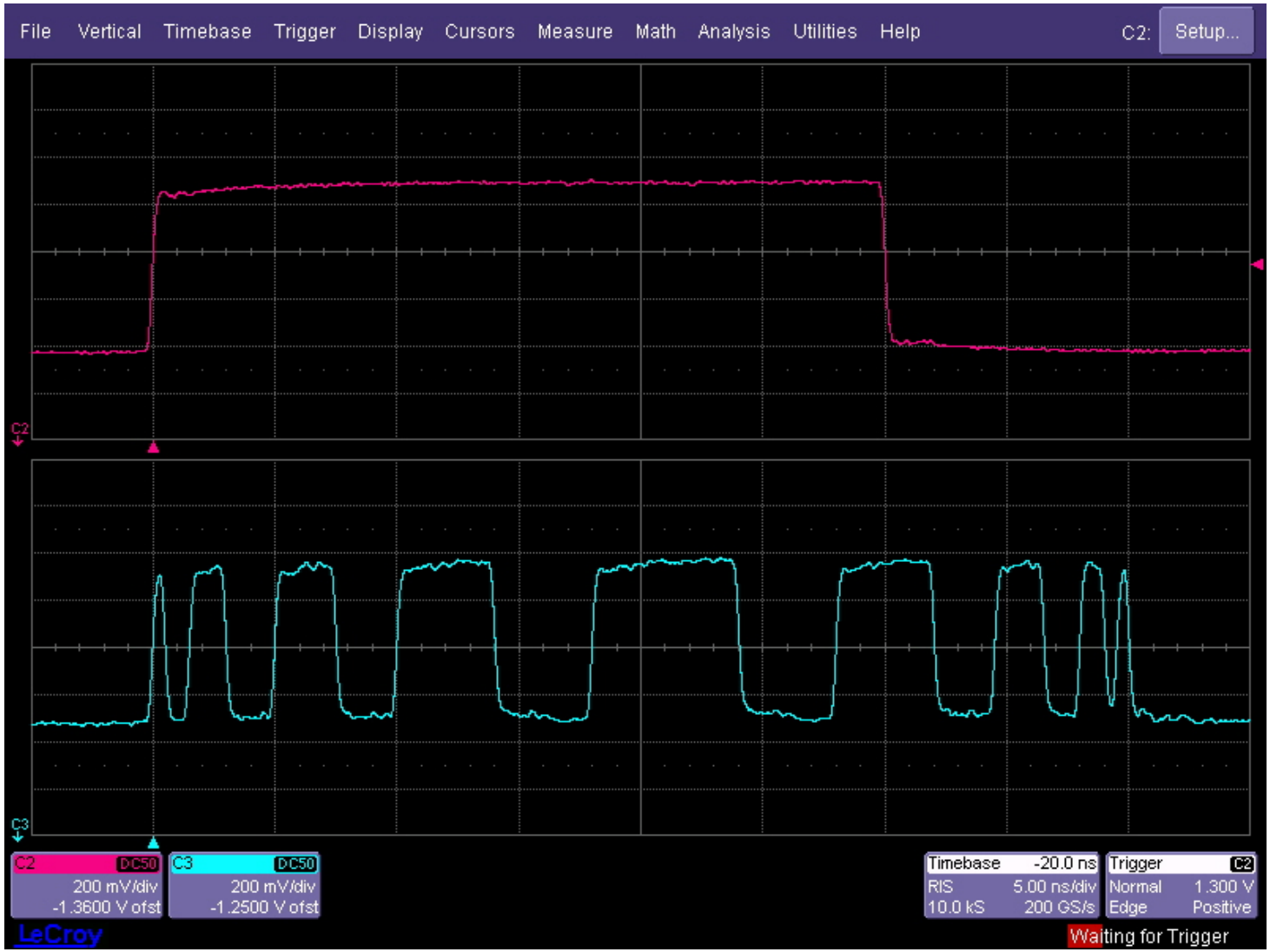
CML pattern outputs (VME-EVR-230RF)



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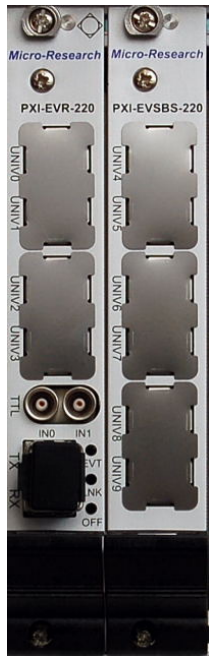
CompactPCI Event Receiver (cPCI-EVR-220)

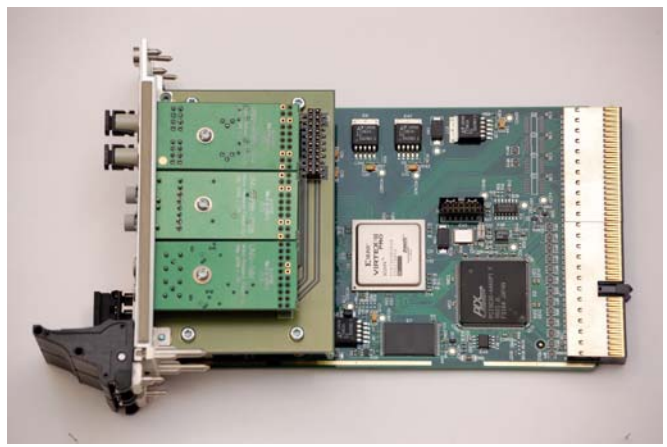
Two Universal I/O slots
• Up to four programmable I/O, TTL/NIM/Optical

• External trigger input
• External inhibit input

SFP transceiver
• Optical signal from EVG (or fan-out)



Optional side-by-side I/O extension module for three Universal I/O slots, providing up to six I/O TTL/NIM/Optical



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Register Map Changes

- CompactPCI boards implement new register mapping
  - Direct addressing of registers, sequencer memories, etc.
  - One type of EVR pulse output:
    - Registers for delay, width, prescaler with SW probable width
    - No more PDP, OTP, TEV, LVL outputs
  - 128 bit wide mapping RAM:
    - 32 bits reserved for internal functions, heartbeat, fifo event, etc.
    - 32 bits for triggering pulses
    - 32 bits to set pulse output
    - 32 bits to reset pulse output
    - No overlapping mapping bits
  - Mapping registers for HW inputs and outputs
  - EVG interrupt support
- Will be available for VME/PMC versions later

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VME-ADC-200 4 x 1 Gsps ADC Prototype

- Designed to be used for filling pattern feedback at SLS
- Two Atmel AT84AD001B Dual 8-bit 1 Gsps ADCs
  - 2 Gsps in interleaved mode
  - 500 mVpp Differential Analog Input
  - 1.5 GHz Full Power Input Bandwidth (-3 dB)
  - Sample clock can be shifted in 10 ps steps
- Integrated Event Receiver
  - Production version will recover RF (ADC conversion clock) from event system
  - Timing/triggering from event system

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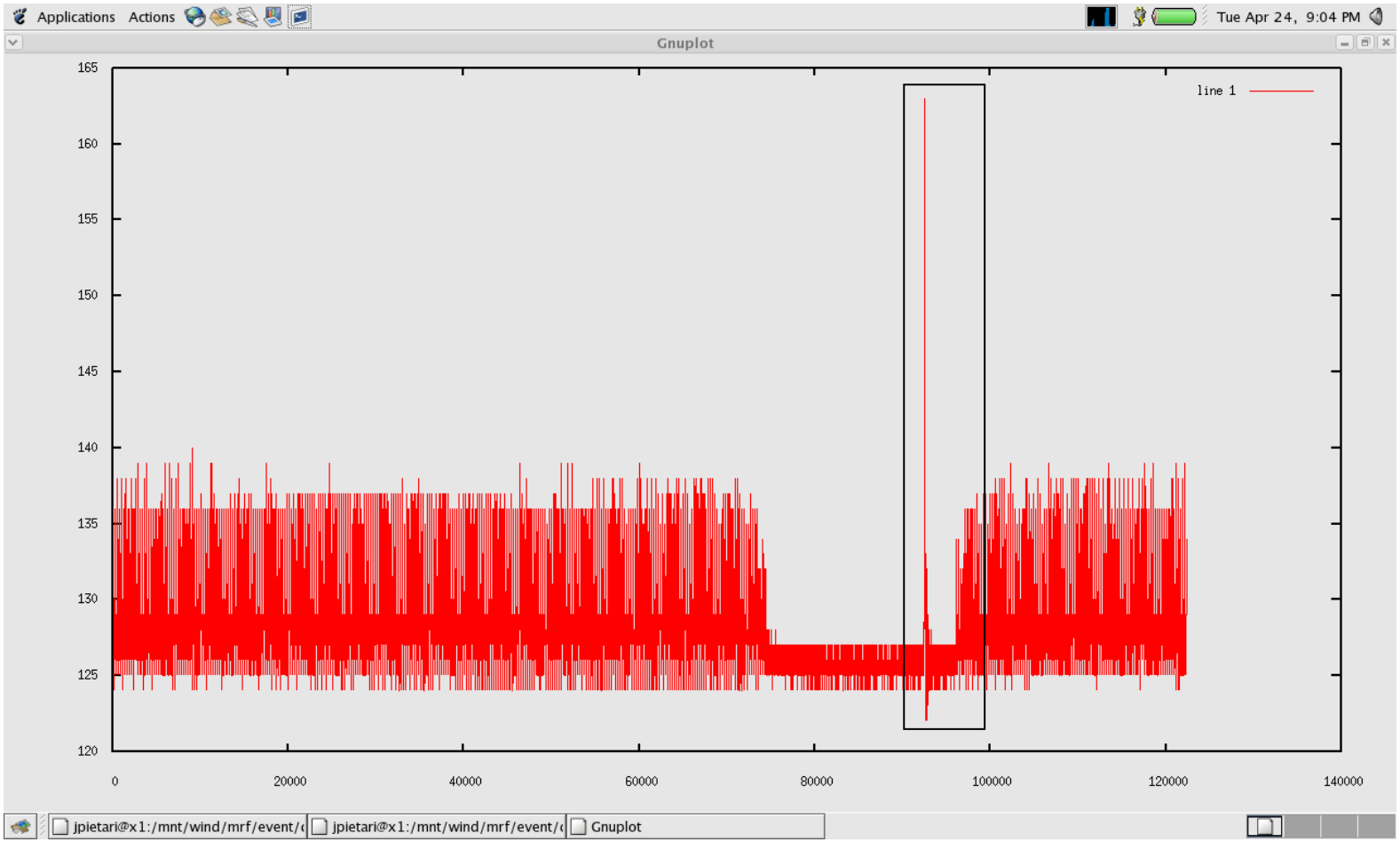
SLS filling pattern sample with VME-ADC-200 prototype



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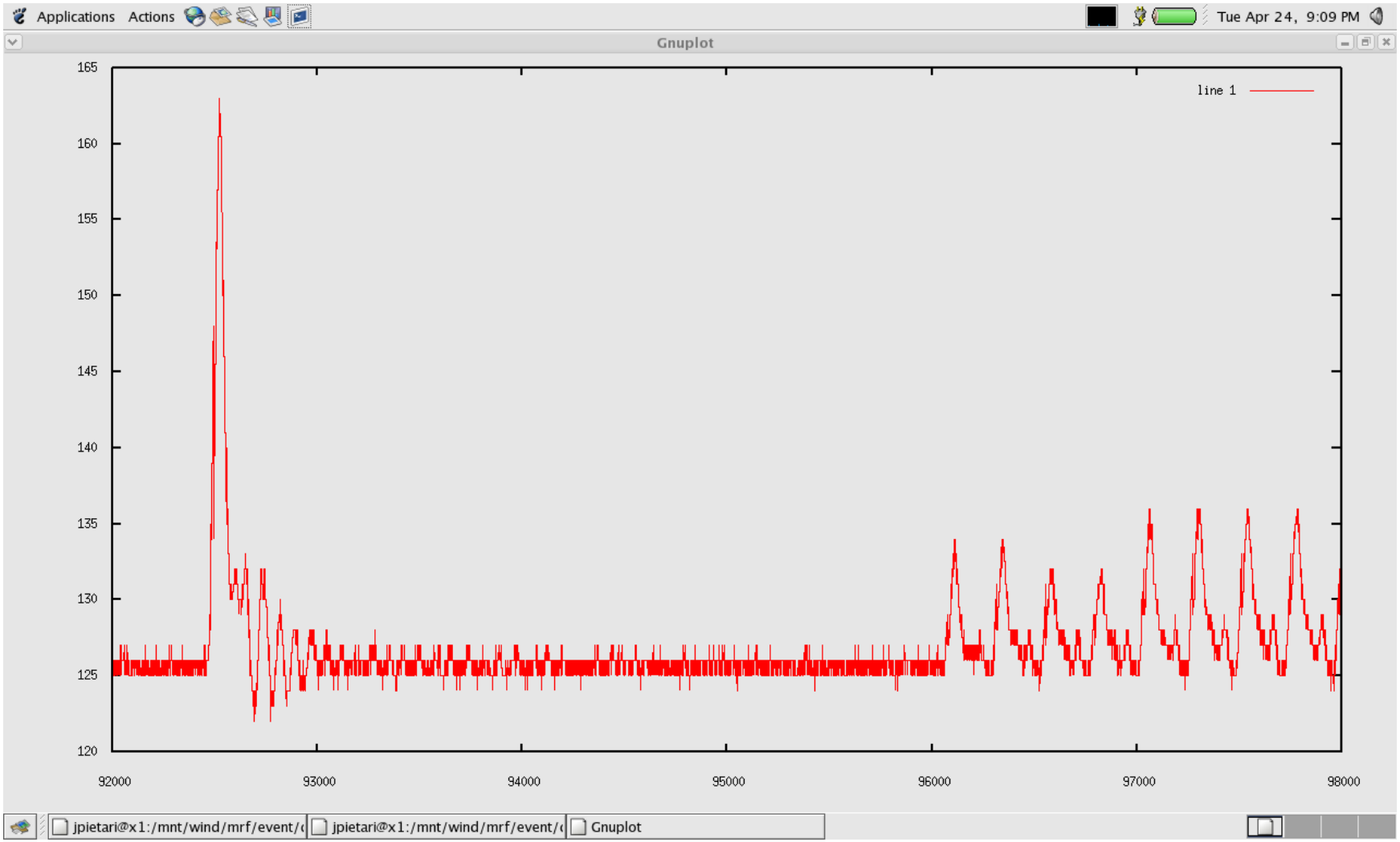
SLS filling pattern sample with VME-ADC-200 prototype



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Future Plans

- VME-EVR/Timer/GunTx Combo
  - To replace 4CHTIM, GUN-TX
  - Up to seven output channels with 10 ps delay resolution
  - LVPECL outputs/two optical outputs for gun driver
  - Integrated EVR
- CompactPCI full speed (2.5 Gbit/s, 125 MHz event clock) versions
  - cPCI-EVG-230
  - cPCI-EVR-230
- CompactPCI EVR/Timer/GunTx Combo
  - Up to three output channels with 10 ps delay resolution
- Introduction of Fan-Out/Concentrator Module
  - Return channel EVR → EVG
  - Interlock operation, EVR reverse heartbeat

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