Open Source Device Control Platform

or

Concept for NSLS2 Fast Orbit Feedback Communications

EPICS Collaboration Meeting, Knoxville, October 2007
Larry Doolittle, LBNL

- **Task:**
  Interconnect ∼180 BPMs and ∼60 corrector magnets to support medium speed orbit feedback.

$$\Delta M = \mathbf{A}\Delta B$$

  where ΔB is the vector of measured beam position errors, and ΔM is the vector of updated corrections to corrector magnets. Thus $\mathbf{A}$ is a 60×180 matrix. Want a system that incorporates strong synchronism and low latency techniques, nominal goal is 200 μs from BPM reading to corrector magnet setting, to support 500 Hz closed-loop bandwidth.

- **Precept (stolen from a 1993 JLab essay):**
  System should be designed for the lowest possible cost, including installation and operation, consistent with reliable, high performance operation.

  Quote from Tom Shea: in a properly designed accelerator, there are no surprises.

  Asynchronism turns into jitter turns into noise. Multiple clock domains, interrupts, and cache all cause jitter.

- **Thought process:**

  NSLS2 is designed to have 30 sectors, each with 6 BPMs and 2 correctors.

  I assert that one BPM's reading can be condensed (for the purposes of fast orbit feedback) to about 64 bits: 24 bits each for X and Y, and 16 bits of status and/or beam current.

  One sector's worth of BPM readings only takes 3.84 μs to move over 100 MB/s Ethernet, which is the slowest plausible chassis-friendly communication medium. It's hard to argue with $5.53 physical layer chips and CAT5 cabling.

  Inter-sector communications should presumably use fiber. Low-end commodity SFP (small-form-factor pluggable) optical modules support 1 to 2 Gbit/s communication rates. At 1 Gbit/sec, the whole ring's worth of BPM data can run down a single fiber in 11.52 μs.

  Can system latency goals be met using this communication gear, when computer networks built with this stuff have trouble scratching their nose in 200 μs?

  The physical layer by itself doesn't add much latency:
  - DP83849C in RMII mode adds 11 bits Tx latency, 38 bits Rx, total 600 ns.
  - XC5VLX MGT adds 6 cycles Tx latency, 11 cycles Rx, total 136 ns at 1 Gbit/sec.

August 2006

National Semiconductor

DP83849C PHYTER® DUAL Commercial Temperature Dual Port 10/100 Mb/s Ethernet Physical Layer Transceiver

General Description

The number of applications requiring Ethernet Connectivity continues to expand. Along with this increased market demand is a change in application requirements. Where single channel Ethernet used to be sufficient, many applications such as wireless remote base stations and industrial networking now require DUAL Port functionality for redundancy or system management.

The DP83849C is a highly reliable, feature rich device perfectly suited for commercial or industrial applications enabling Ethernet on the factory floor. The DP83849C features two fully independent 10/100 ports for multi-port applications.

The DP83849C provides optimum flexibility in MPU selection by supporting both MII and RMII interfaces. In addition this device includes a powerful new diagnostics tool to ensure initial network operation and maintenance. In addition to the TDR scheme, commonly used for detecting faults during installation, NATIONAL's innovative cable diagnostics provides for real time continuous monitoring of the link quality. This allows the system designer to implement a fault prediction mechanism to detect and warn of changing or deteriorating link conditions.

With the DP83849C, National Semiconductor continues to build on its Ethernet expertise and leadership position by providing a powerful combination of features and flexibility, easing Ethernet implementation for the system designer.

Features

- **Low-power 3.3V, 0.18µm CMOS technology**
- **Low power consumption <600mW Typical**
- **3.3V MAC Interface**
- **Auto-MDIX for 10/100 Mb/s**
- **Energy Detection Mode**
- **Dynamic Integrity Utility**
- **Dynamic Link Quality Monitoring**
- **TDR based Cable Diagnostic and Cable Length Detection**
- **Optimized Latency for Real Time Ethernet Operation**
- **Reference Clock out**
- **RMII Rev. 1.2 Interface (configurable)**
- **SNI Interface (configurable)**
- **MII Serial Management Interface (MDC and MDIO)**
- **IEEE 802.3u MII**
- **IEEE 802.3u Auto-Negotiation and Parallel Detection**
- **IEEE 802.3u ENDEC, 10BASE-T transceivers and filters**
- **IEEE 802.3u PCS, 100BASE-TX transceivers and filters**
- **Integrated ANSI X3.263 compliant TP-PMD physical sub-layer with adaptive equalization and Baseline Wander compensation**
- **Programmable LED support for Link, 10 /100 Mb/s Mode, Activity, Duplex and Collision Detect**
- **Single register access for complete PHY status**
- **10/100 Mb/s packet BIST (Built in Self Test)**
- **80-pin TQFP package (12mm x 12mm)**

Applications

- Medical Instrumentation

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- Cisco 10G

Fortune 50 Approved

More Detail

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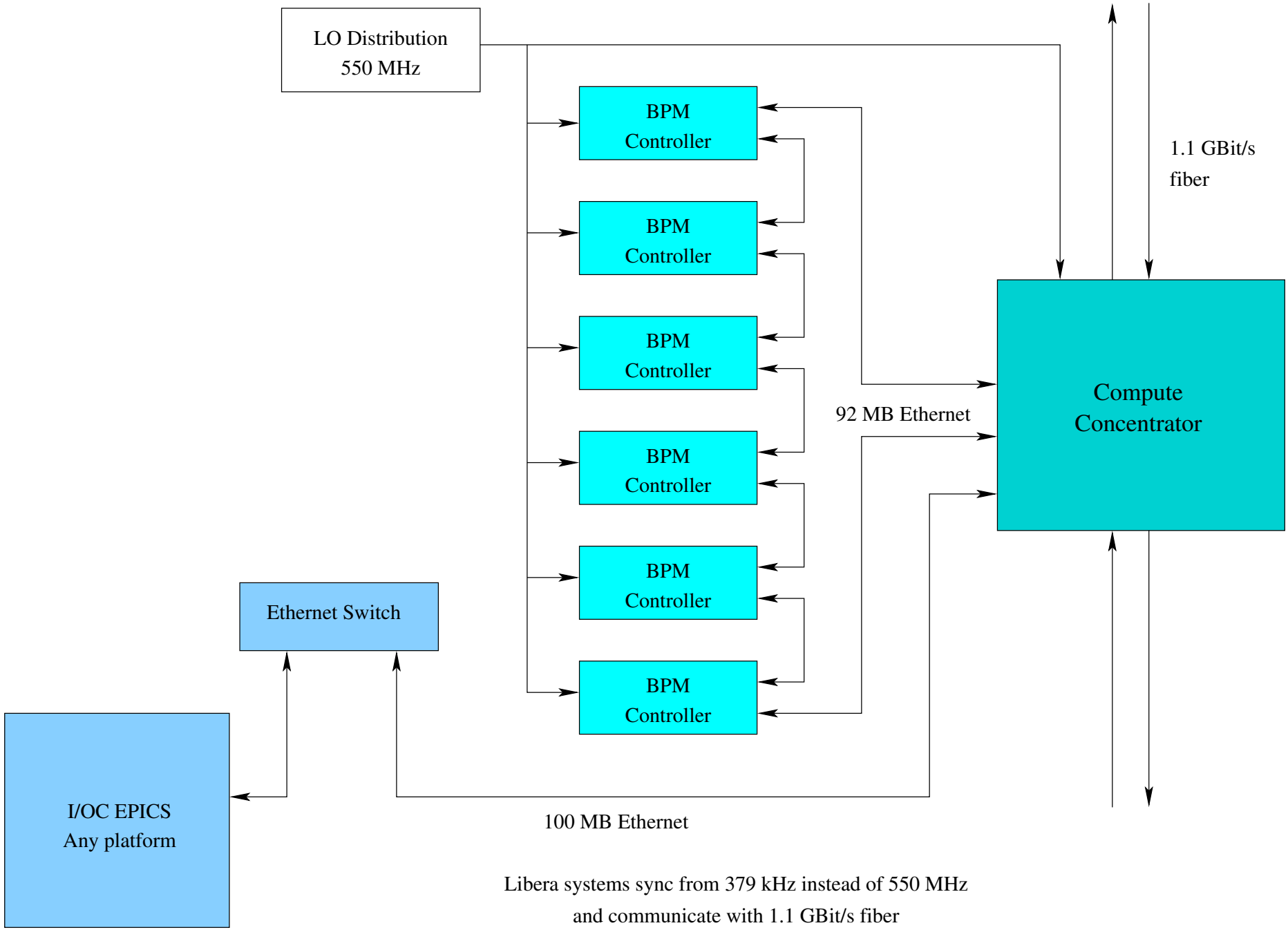

Libera systems sync from 379 kHz instead of 550 MHz
and communicate with 1.1 GBit/s fiber

Virtex-5 Family Overview
LX, LXT, and SXT Platforms

DS100 (v3.0) February 2, 2007

Advance Product Specification

General Description

The Virtex™-5 family provides the newest most powerful features in the FPGA market. Using the second generation ASMBL™ (Advanced Silicon Modular Block) column-based architecture, the Virtex-5 family contains four distinct platforms (sub-families), the most choice offered by any FPGA family. Each platform contains a different ratio of features to address the needs of a wide variety of advanced logic designs. This overview contains detailed information about the LX, LXT, and SXT platforms. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices, SelectIO™ technology with built-in digitally-controlled impedance, ChipSync™ source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated DCM (Digital Clock Managers) and phase-locked-loop (PLL) clock generators, and advanced configuration options. The LXT and SXT devices also contain power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, a PCI Express™ compliant integrated Endpoint block, and tri-mode Ethernet MACs (Media Access Controllers). These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. Most advanced system designs require the programmable strength of FPGAs. Virtex-5 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities. The Virtex-5 LXT, SXT, and FXT platforms include advanced high-speed serial connectivity and link/transaction layer capability.

Summary of Virtex-5 Features

- Four platforms LX, LXT, SXT, and FXT
  - Virtex-5 LX: High-performance general logic applications
  - Virtex-5 LXT: High-performance logic with advanced serial connectivity
  - Virtex-5 SXT: High-performance signal processing applications
  - Virtex-5 FXT: High-performance embedded systems
- Cross-platform compatibility
  - LXT, SXT, and FXT devices are footprint compatible in the same package
- Most advanced, high-performance, optimal-utilization,
- High-performance parallel SelectIO technology
  - 1.2 to 3.3V I/O Operation
  - Source-synchronous interfacing using ChipSync technology
  - Digitally-controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support
- Advanced DSP48E slices
  - 25 x 18, two's complement, multiplication
  - Optional adder, subtracter, and accumulator
  - Optional pipelining
  - Optional bitwise logical functionality

- **High performance with commodity network hardware:**
  - Yes, if computers delegate the real-time work to FPGAs.
  - Ideally all clock sources are coherent, allows "perfect" interval measurement by cycle counting.

- **Potential Clients for a real-time beam dynamics network:**
  - BPM
  - Correctors
  - LLRF
  - Transverse Feedback
  - Longitudinal Feedback
  - Machine Protection

- **EPICS hookup:**
  - EPICS on FPGA performance will lag that of a "real" computer
  - FPGAs are generally used for high performance front ends
  - putting the CPU in the critical path is not a good match
  - Prefer a UDP/IP protocol for smooth FPGA implementation and clean hookup to an EPICS gateway
  - FPGA-based network attachment will allow 1μs latency and 20 ns time stamps, instead of $> 100\mu$s.

- **Platforms:**
  - Commercial Evaluation boards for early code development
  - Libera?
  - LLRF4 - expanded to include Ethernet "open source"
  - Could make a PMC client, could participate in the network but of course the hard-real-time character disappears crossing the PCI bus to a conventional computer

Cost outline

- **Addition per leaf:**

(assuming a $40+ class FPGA is already on board with 17 pins available)

National DP83849C dual ETH PHY	$5.53
Pulse J8064D628A dual RJ-45 w/magnetics	$6.89
Passives, board area, assembly	$10.00
total:	about $22.00

- **Concentrator nodes:**

Virtex-5 LXT FPGA:	at least $333.00
2 x 2GBit/s SFP:	$116.00
3 x National DP83849C dual ETH PHY	$16.59
3 x Pulse J8064D628A dual RJ-45 w/magnetics	$20.67
Other components	$60.00
Board fabrication (6-layer 100 x 150 mm)	$150.00
Assembly	$300.00
total	about $1000.00

- **Software and engineering:**

priceless

Conclusions

- FPGAs enable orders of magnitude improvement in latency and timing precision
- Hardware is (nearly) *gratis*, software is expensive
- Smooth interconnect with commodity hardware and upper levels of software will be a challenge
- Promising work going on in many labs – need to build more collaborations,
- We need more more FPGA experts!