Timing goes Express

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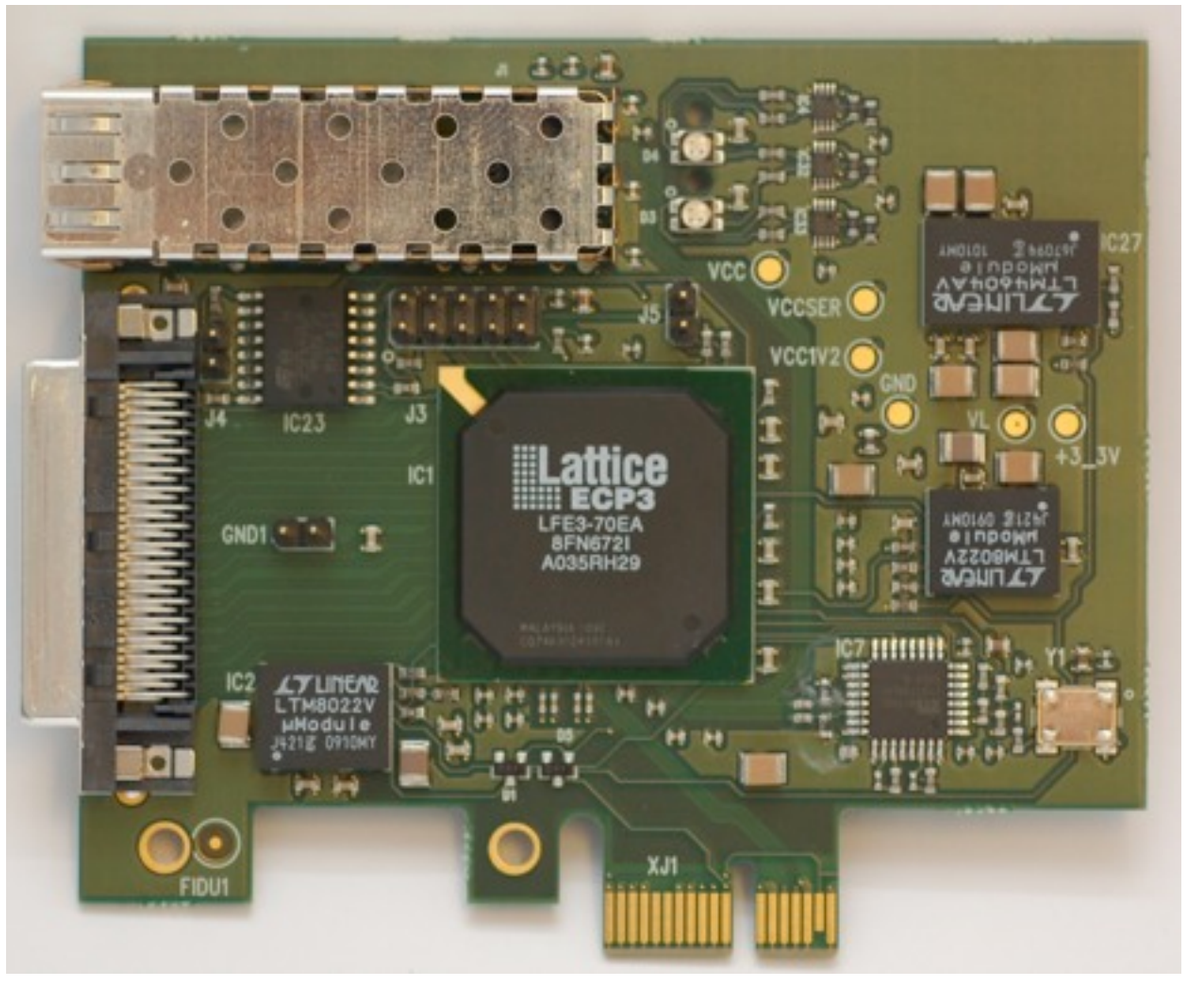
PCIe-EVR-300

- Based on cPCI-EVR-300 design
  - –PCI replaced with PCIe (Lattice IP core)
  - –Lattice ECP3 FPGA
  - –I/O on VHDCI connector
  - –SFP transceiver
  - –two RGB LEDs
  - –91.7 mm x 79.2 mm
  - –14 layer PCB



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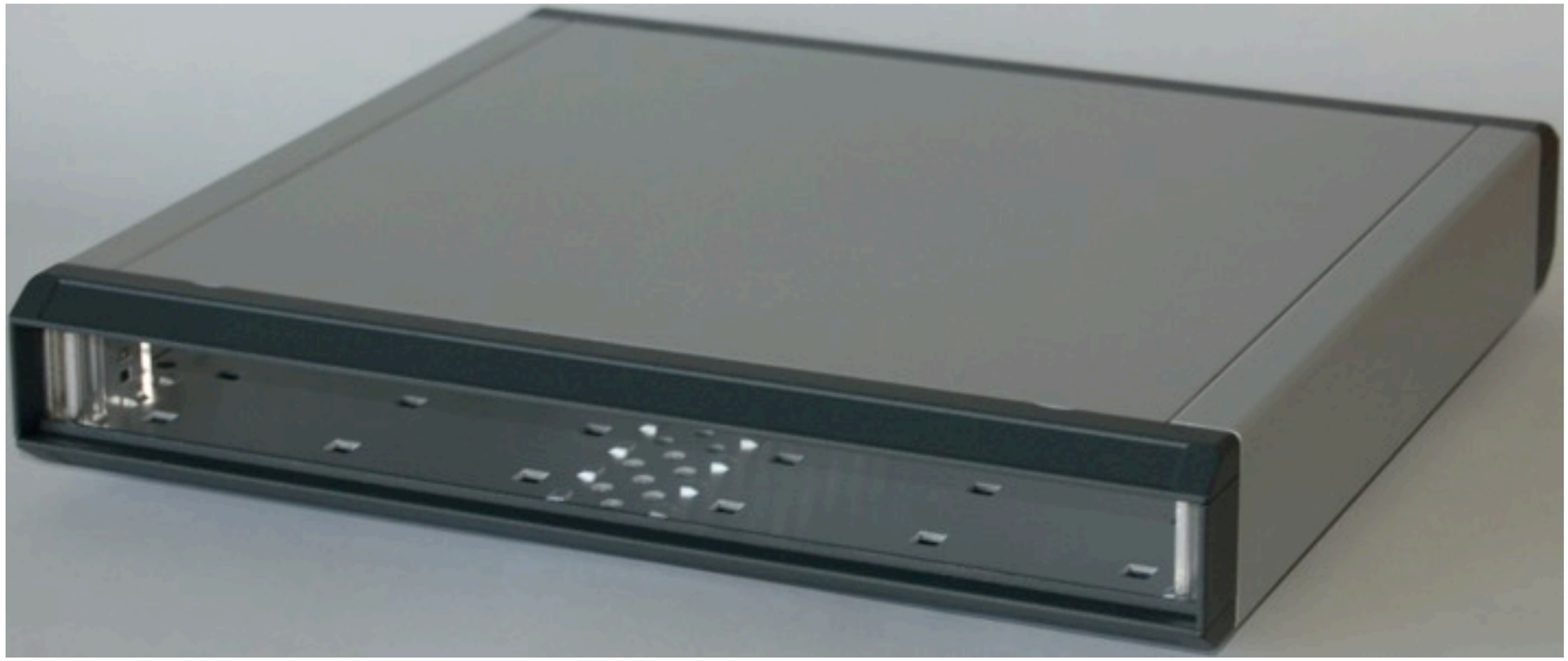
Interface Board IFB-300

- Schroff 24572-100 ratiopacPRO case
  - 42.5 mm high, 255.5 mm deep
  - Holds one 6U PCB
- Eight Universal I/O slots
- Four indicator LEDs
- 19” Rack mount brackets available



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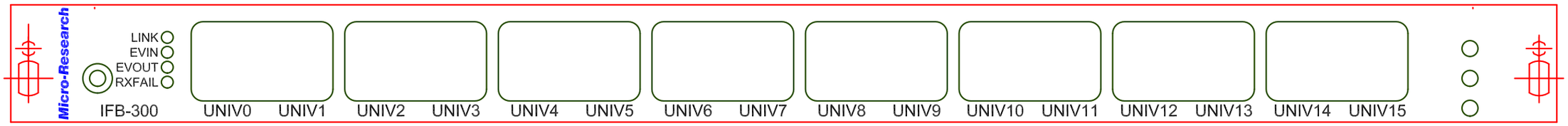
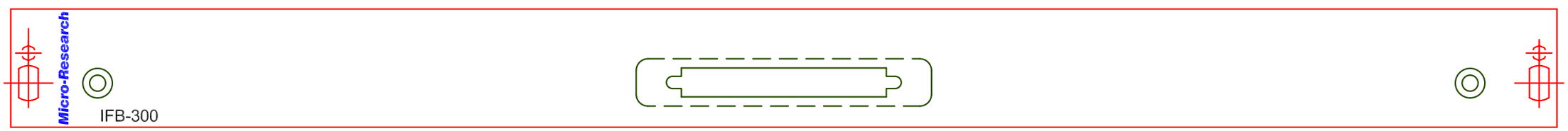
Interface Board IFB-300



–Front side has a handle on the right hand side

–To replace I/O modules one has to take off back side VHDCI connector screws and loosen front panel fastening screws. PCB will slide out.



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PCIe-EVR Current Status

- Prototype batch assembled in June, minor issues resolved
- First small production batch is being assembled in a few weeks
- Mechanic parts (IFB cases, panels, PCIe bracket, IFB rack mounting bracket) are available
- First production units will ship in November 2011

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PCIe-EVR-300 versus Prototype

- Re-configuration cannot be initiated by PCI Express reset signal, configuration has to start immediately after power up
- DLS insisted on having an external CDR on the production version, however, the CDR (with bandwidth limit of 2.7 Gbps) can be bypassed
  - DLS wants to cascade EVRs and this does not work unless signal is regenerated through a CDR

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PCIe-EVR Lessons Learned

- PCI Express is not a drop-in replacement for conventional PCI in FPGAs
- Requires wrapper between PCI Express core transaction layer and FPGA peripheral bus (Wishbone, OPB, PLB).
- FPGA vendors provide interfaces between the PCI Express transaction layer and FPGA system bus
- On software side there is no difference between PCI / PCI Express
- Hardware layout is much simpler, only three differential pairs between FPGA and PCI Express connector, reference clock, TX and RX
- One has to pay attention to FPGA configuration time

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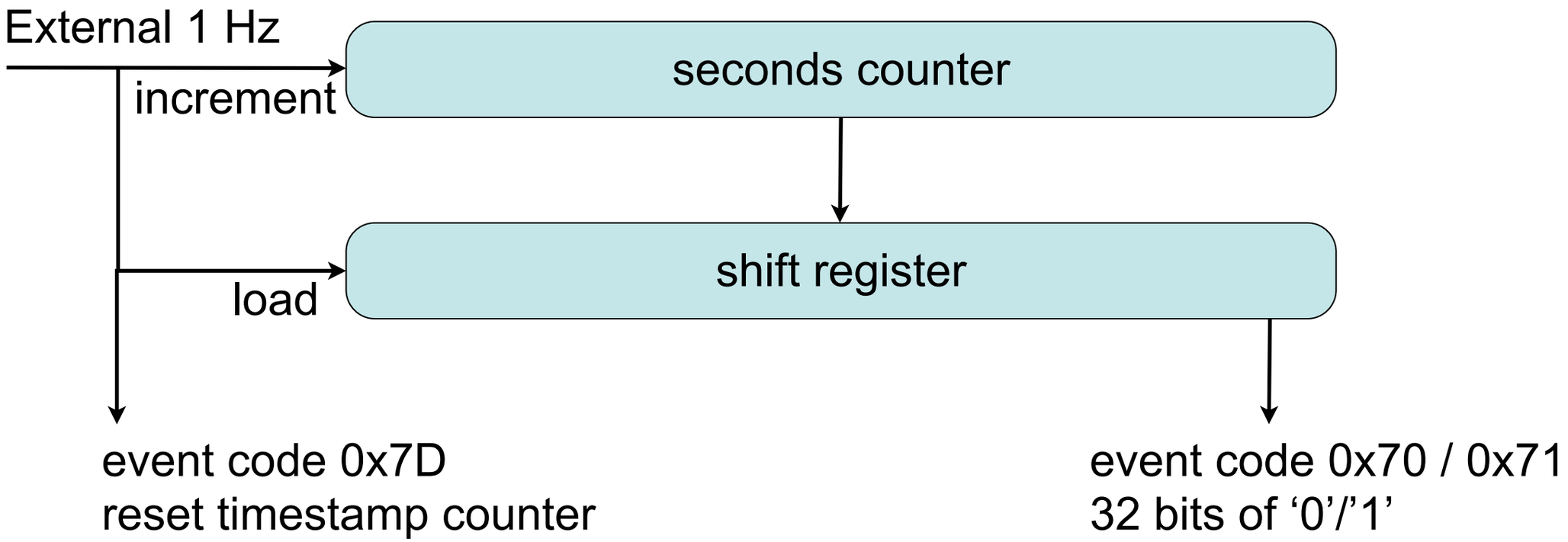
Timestamping Improvements (for TPS)

- Seconds logic in FPGA for automatic timestamp event generation in EVG with externally supplied 1 Hz/1 MHz clocks



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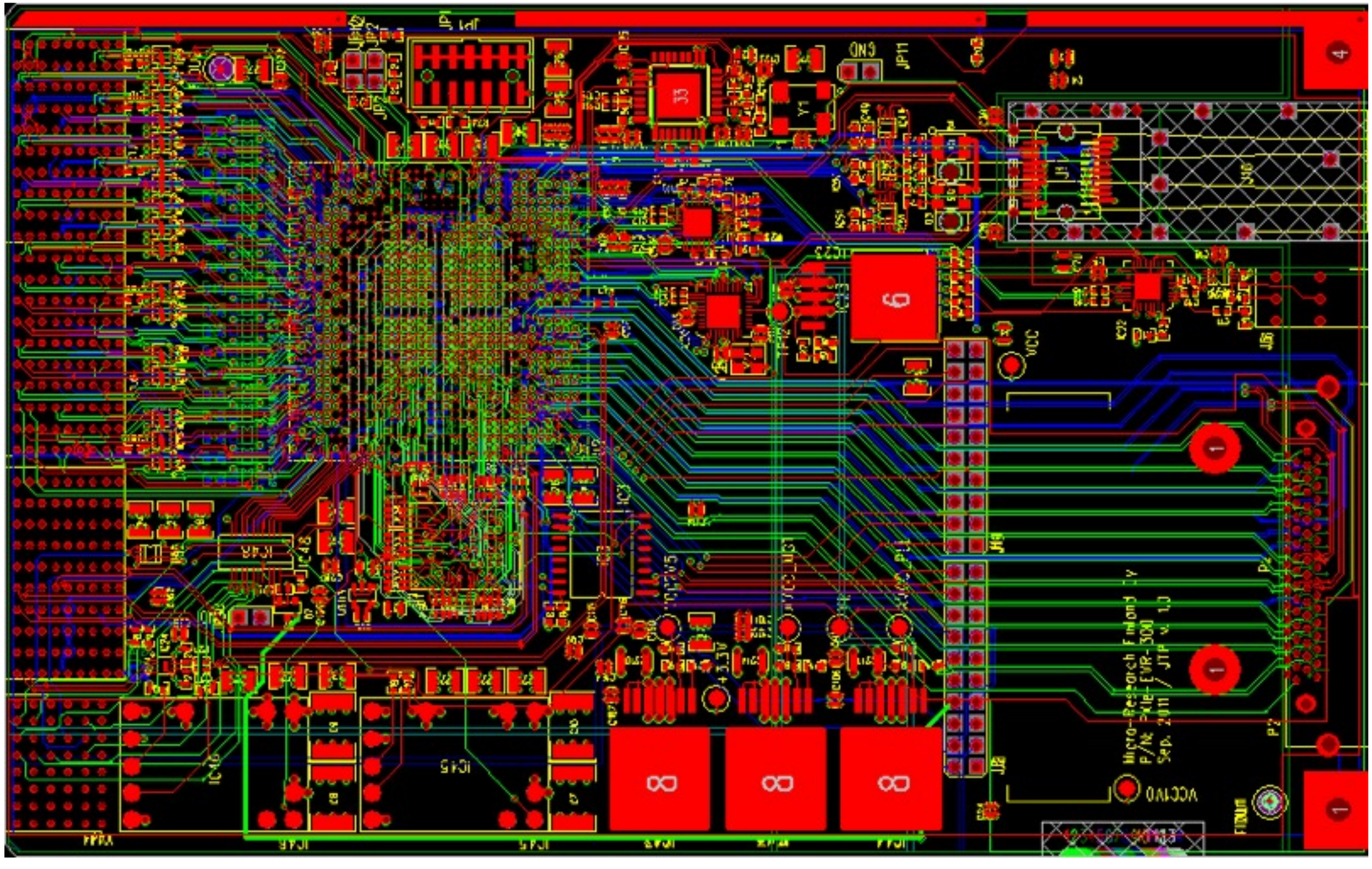
PXIe-EVR-300 Prototype Design

- An Event Receiver for the PXIe System Timing Slot



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PXIe-EVR-300 Prototype Design - Features

- Eight bit PXI trigger bus
- 17 Star triggers, one to each individual slot
- 3 x 17 Differential lines, three to each individual slot
  - –one clock signal DSTARA from EVR to peripheral
  - –one trigger signal DSTARB from EVR to peripheral
  - –one signal DSTARC from peripheral to EVR
- Capability to provide 10 MHz reference to backplane (backplane generates 100 MHz from 10 MHz)
- Two front panel TTL inputs
- Two front panel Universal I/O slot (optionally connection to Interface board IFB-300 with eight Universal I/O slots)

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PXIe-EVR-300 Prototype Design - Features

- New clock cleaner circuit / no external CDR between SFP and FPGA
  - –also to study new ways to design a fan-out for operation above 2.7 Gbps
- Prototype EVG features - Reference clock sources
  - –fractional synthesizer
  - –10 MHz PXI reference clock from backplane multiplied/cleaned to e.g. 100 MHz or 125 MHz
  - –100 MHz from backplane
  - –Front panel RF input similar to EVG

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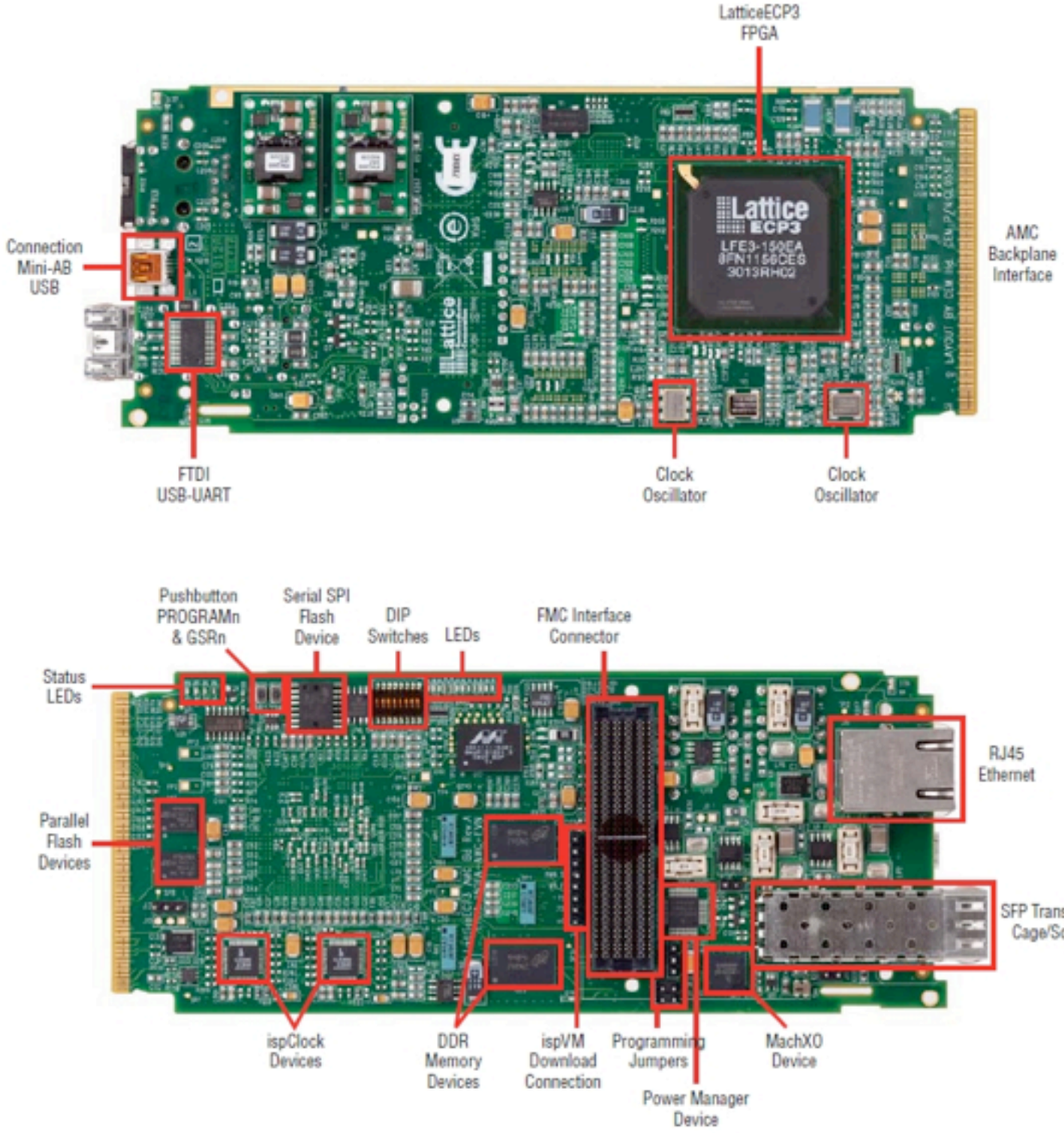
AMC-EVR Plans

- Lattice has recently released an AMC Evaluation platform based on a ECP3 FPGA
- Good starting point for AMC-EVR following MTCA.4 (microTCA for Physics)



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Future Plans - Requirements of SwissFEL

- Sequencer changes
  - –multiple sequences with user defined playback order (would BNL sequencer code be usable?)
- Higher event rate/bit rate 142.8 MHz (2.856 Gbit/s)
- Increase precision of sequence trigger delay/phase shifter
- Another way of timestamping:
  - –multiplexed counter with fractional part that will allow for fine tuning of timestamp resolution

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Future Plans - Requirements of SwissFEL

- Higher event rate/bit rate 142.8 MHz (2.856 Gbit/s)
  - –most challenging requirement
  - –current CDRs go only up to 2.7 Gbit/s
  - –omit CDRs in fan-outs?
  - –regenerate event clock at fan-out
    - will add delay of 100-200 ns fan-out level
    - lots of possibilities
      - –insert events

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Future Plans

- PXIe-EVR
- AMC-EVR
- new higher speed VME-EVG / VME-EVR / fan-out
- new VME-ADC digitizer

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