INTRODUCE OF SINAP TIMING SYSTEM

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SINAP
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History of SINAP timing system development

- Starting to learn event timing system in 2003.
- Implementing MRF serials 200 modules in SSRF timing system in 2007.
- Starting to design first prototype (virtex-4) in Oct. 2009.
- Finishing version 1 development in Sep. 2010, the RMS jitter is less than 9ps.
History of SINAP timing system development

• Starting version2 development in Feb 2011
• VME-EVE prototype in July 2011
• VME-EVO prototype in Nov 2011
• Finishing VME-EVE and VME-EVO development in May 2012
• Finishing PLC-EVR and STD-OE development in Sep 2012
• RMS jitter of version2 system is less than 7ps
version1 system structure
Features of version1 system

- Classic star broadcast network
- Fiber link is 2.5Gbit/s
- Event clock is 120 - 135MHz
- Hardware is based on Virtex-4 FPGA and CPLD
- Standard 6U VME module
- Fiber output in EVR has 1/20 event clock delay and 5ps delay
- Hardware interlock function in EVR
- Interrupt functions are supported in EVG and EVR
Version 1 modules and detail

EVG
EVR
FANOUT
TTL VME Transition Board
Plastic fiber VME Transition Board
Multimode fiber O/E
Plastic fiber O/E
EVG

VME 6U module, A16D32 addressing
Input: 1ch RF clock (0 – 10dBm)
       1ch AC line (3Vp-p typical)
Output: 1ch multi-mode fiber
        1ch Sequence RAM trigger (TTL)
EVR

VME 6U module, A16D32 addressing
Input: 1ch multi-mode fiber
1ch interlock input (TTL)
Output: 3ch TTL trigger/clock(50ohm)
3ch LVPECL trigger/clock
1ch CML RF recovery clock
2ch Multi-mode fiber trigger
FANOUT

VME 6U module
Input: 1ch multimode fiber
Output: 12ch multimode fiber
TTL VME Transition Board

VME transition board
Output: 14ch TTL trigger (50ohm)
Plastic Fiber VME Transition Board

VME transition board
Output: 14ch optic trigger
(Agilent HFBR-1528)
Multi-mode Fiber O/E

Standalone module

Input: 1ch multi-mode fiber
1ch power supply (24V/1A)
Output: 1ch TTL (50ohm)

Coupled with EVR
For long distance transmission
Plastic Fiber O/E

Standalone module
Input: 1ch multi-mode fiber
  1ch power supply (24V/1A)
Output: 1ch TTL(50ohm)

Coupled with Plastic Fiber VME Transition Board
For short distance transmission
version 1 system performance

- Event code transmission
coding-decoding error
Performance Testing in PAL lab

- Jitter
  EVR TTL output
  < 6ps
Performance Testing in PAL lab

- **Jitter**
  Multi-mode O/E output < 10ps
  This is the jitter of the tested whole system
Performance Testing

- Phase Shift

Phase shift with temperature changing (35ps/℃)
version 1 application in PLS-II

in LINAC control room

in RF station (EVG)
version1 application in PLS-II
version1 application in PLS-II
version1 software

• Based on EPICS base 3.14.8.2 and vxWorks 5.5.1
• During injection, the positions of all injection event codes stored in Sequence RAM of EVG will be changed, but delay values of EVR output keep fixed.
• When all event codes are transmitted, an interrupt will be generated in EVG, which makes a new event codes’ list added to Sequence RAM.
• This mechanism is easy and efficiency.
SINAP v2 timing system structure
Features of version 2 system

- Classic start network
- Bidirectional event frame transfer (not broadcast)
- Fiber link is 2.5Gbit/s
- Event clock is 120 - 135MHz
- Hardware is based on Virtex-6 FPGA
- Standard 6U VME module
- Adding PLC-EVR based on Yokogawa F3RP61 series
Features of version2 system

- Jitter performance improved based on redesigned hardware circuits
- Types of modules simplified
- VME-EVO configured as EVG, EVR or FOUT by software
- All clocks generated in EVR; distributed bus abandoned
- Date duplex transfer supported
- All outputs delay resolution event clock, 1/20 event clock and 5ps time step
version2 hardware

VME-EVO
VME-EVE
PLC-EVR
STD-OE
VME-EVO

Configured to EVG, EVR and FANOUT by software
VME 6U module, A16D32 addressing
Input: 1 RF clock (0 – 10dBm) (50MHz~1300MHz)
    1 interlock / AC-line (TTL)
    1 fiber (SFP module)
Output: 8 fiber (SFP module)
VME-EVO (Configured to EVG)

- **Uplink**: SFP → GTX → event FIFO
- **Data Switching**: GTX0 → SFP0 → EVG logic → data FIFO
- **Downlink**: Recovery clock → AC line → RF clock → GTX1 → SFP1 → data Switching
- **GTX7**: SFP7 → ……

Diagram:
- SFP
- GTX
- event FIFO
- data FIFO
- EVG logic
- data Switching
- GTX0
- SFP0
- GTX1
- SFP1
- ……
- GTX7
- SFP7
- Recovery clock
VME-EVO (Configured to FANOUT)

VME-EVO (Configured to FANOUT) Diagram:
- Uplink: SFP to GTX
- Recovery clock: GTX to SFP
- Downlink: GTX to SFP
- Data switching: GTX to GTX

Components:
- GTX0 to GTX1 to GTX7
- SFP0 to SFP1 to SFP7
VME-EVO (Configured to EVR)
VME-EVE (only Configured to EVR)

VME 6U module, A16D32 addressing

Input: 1 interlock (TTL)
     1 fiber (SFP module)

Output: 8 outputs (TTL)
     1 RF recovery clock
VME-EVE

Diagram:

- Uplink
- SFP
- GTX
- EVR logic
- Data logic
- Recovery clock
- GTX8
- GTX0
- GTX1
- GTX7
- GTX8
- GTX0
- GTX1
- GTX7
- RF transformer
- Fine delay
- RF
- TTL
- TTL
- TTL
- TTL
VME-EVE

- RF recovery clock can be set into anyone of five clocks
  1 -> event clock
  2 -> 2x event clock
  3 -> 4x event clock
  4 -> 5x event clock
  5 -> 10x event clock
VME-EVE

- RF delay

(Synchronized with RF clock)
(Resolution: 1/20 event clock)
PLC-EVR

Yokogawa FAM3 series, 1-slot module
Input/Output register mode
external 5V/3A DC power supply
Input: 1 fiber (SFP module)
Output: 4 TTL outputs (50ohm)
STD-OE

19 inches 1U standard chassis
110/220V 50-60Hz AC power supply
Input: 4 fiber (SFP module)
Input: 4 independent Interlocks
Output: 4 outputs (TTL)
Coupled with VME-EVO (configured to EVR)
For long distance transmission
Performance test at KEK lab

- Jitter
  EVE TTL output
  < 7ps
Performance test at SINAP lab

- Jitter

VME-EVE

TTL output < 5.5 ps
Performance test at SINAP lab

- Jitter
  - PLC-EVR
  - TTL output < 5.9 ps
Conclusion

• version1 modules is already stable used in PLS-II
• version2 hardware development was finished, also software could be supported later.
• In future, version2 may implement in many project. SuperKEKB China ADS Shanghai Proton Therapy Project ……