Fast Orbit Feedback System for NSLS-II

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NSLS-II Controls Group

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Outline

1. About NSLS-II
2. Technical Requirement and cell structure
3. Fast Orbit Feedback overview
4. Hardware for FOFB
   • Beam Position Monitor (BPM)
   • Corrector Power Supply Controller
   • Cell Controller (CC)
   • Timing synchronization
5. FOFB System
   • Feedback Algorithm
   • Feedback Implementation
   • EPICS IOC configuration
6. Status and Plan
7. Summary
About NSLS-II (http://www.bnl.gov/ps/nsls2/about-NSLS-II.asp)

**Purpose**
- To provide extremely bright x-rays for basic and applied research in biology and medicine, materials, chemical sciences, geosciences, environmental sciences, and nanoscience

**Sponsor**
- U.S. Department of Energy (DOE), Office of Science, Office of Basic Energy Sciences

**Costs**
- $912 million to design and build

**Features**
- State-of-the-art, medium-energy (3 GeV) electron storage ring that produces x-rays up to 10,000 times brighter than the NSLS

**Users**
- Researchers from around the world
## Technical Requirement & Specifications

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy</td>
<td>3.0 GeV</td>
</tr>
<tr>
<td>Circumference</td>
<td>792 m</td>
</tr>
<tr>
<td>Number of Periods</td>
<td>30 DBA</td>
</tr>
<tr>
<td>Length Long Straights</td>
<td>6.6 &amp; 9.3m</td>
</tr>
<tr>
<td>Emittance (h,v)</td>
<td>&lt;1nm, 0.008nm</td>
</tr>
<tr>
<td>Momentum Compaction</td>
<td>0.0037</td>
</tr>
<tr>
<td>Dipole Bend Radius</td>
<td>25m</td>
</tr>
<tr>
<td>Energy Loss per Turn</td>
<td>&lt;2MeV</td>
</tr>
<tr>
<td>Energy Spread</td>
<td>0.094%</td>
</tr>
<tr>
<td>RF Frequency</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Harmonic Number</td>
<td>1320</td>
</tr>
<tr>
<td>RF Bucket Height</td>
<td>&gt;2.5%</td>
</tr>
<tr>
<td>RMS Bunch Length</td>
<td>15ps-30ps</td>
</tr>
<tr>
<td>Average Current</td>
<td>500ma</td>
</tr>
<tr>
<td>Current per Bunch</td>
<td>0.5ma</td>
</tr>
<tr>
<td>Charge per Bunch</td>
<td>1.2nC</td>
</tr>
<tr>
<td>Touschek Lifetime</td>
<td>&gt;3hrs</td>
</tr>
<tr>
<td>Top-Off Injection rate</td>
<td>1/min</td>
</tr>
</tbody>
</table>

### Diagrams

- **Injection System**
- **SR**
BNL site field vibration measurement

Displacement PSDs at locations near the NSLS-II site
(Source: N. Simos)

RMS Displacements at CFN
(0.5-4) Hz : 200 nm
(4-50) Hz : 20 nm
(50-100) Hz : 0.4 nm

NSLS-I X-ray ring (Vertical in Operations since Sept. 2002)
**SR BPMs and Correctors Location**

**Slow correctors (Qty=6)**
- Slow response – 2 Hz
- Strong strength – 800 μrad
- Utilized for –
  - Alignment
  - Slow orbit feedback

**Fast correctors (Qty=3)**
- Fast response – 2 kHz
- Weak strength – 15 μrad
- Utilized for –
  - Fast orbit feedback

156 mm slow
100 mm slow
30 mm fast (air core)
What is Fast Orbit Feedback

- Global orbit correction system for sub-micron orbit stability
- Beam stabilization and high brightness
- Minimize the beam instability from many different noise source
  - Ground settlement, power switching noise, temperature, cooling water, FAN, Insertion device gap change, fill pattern, beam intensity, booster ramp ..,
- Based on Singular Value Decomposition (SVD) algorithm
- Read beam position data every 1 kH ~ 10 kHz
- Calculate new correct kick values for minimization of the RMS orbit
- Update PS set values every 1 kH ~ 10 kHz
- Less then 200 nm orbit stability at 0 Hz – 1 kHz
**NSLS-II Fast Orbit Feedback Specifications**

- Powerful Virtex-6 FPGA based hardware digital signal processor
- Feedback rate: 10 kHz
- Bandwidth: ~2 kHz
- Number of BPMs: 180 ea
  - NSLS-II in house designed Digital BPM
- Number of Correctors: 90 ea
  - 10 ~ 15 urad, 20 bit resolution, 1 ppm response
- Control algorithm: SVD, Individual Eigen mode with PID control
  - FPGA based parallel matrix calculation
- Update correct set values every 10 kHz
  - 5 Gbps fiber optics communication for BPM and CC, 100 Mbps for PS
- Remote firmware upgrade (tftp client/server), 10 miniature per unit, parallel running
Topology of the FOFB network

- 30 cells
- 6 BPMs per sector
- 3 Fast and 6 Slow H/V correctors per sector
- Cell controller distribution takes 15 us
- PS controller distribution takes 5 us

One Cell configuration
BPM

Beam position measurement
## NSLS-II Performance requirement

### Parameters/ Subsystems

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Vertical</th>
<th>Horizontal</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BPM</strong></td>
<td>Data rate = 378 kHz</td>
<td>3 μm rms</td>
</tr>
<tr>
<td><strong>Receiver</strong></td>
<td>0.017 Hz to 200 Hz</td>
<td>0.2 μm rms</td>
</tr>
<tr>
<td><strong>Electronics</strong></td>
<td>200 Hz to 2000 Hz</td>
<td>0.4 μm rms</td>
</tr>
<tr>
<td><strong>Turn by Turn (80% fill)</strong></td>
<td>1 min to 8 hr drift</td>
<td>0.2 μm rms</td>
</tr>
<tr>
<td><strong>Assuming no contribution from bunch/ fill pattern effects</strong></td>
<td>DC to 2000 Hz</td>
<td>0.2 μm rms</td>
</tr>
<tr>
<td><strong>Mechanical motion limit at Pick-up electrodes assembly (ground &amp; support combined)</strong></td>
<td>Vibrations</td>
<td>50 Hz to 2000 Hz</td>
</tr>
<tr>
<td><strong>50 Hz to 2000 Hz</strong></td>
<td>Thermal</td>
<td>1 min to 8 hr</td>
</tr>
</tbody>
</table>

### Storage Ring

- Frev = 378KHz
- Frf = 499.68MHz

### Injection System

- Frev = 1.89MHz
- Bunch Spacing = 2ns
- Rep Rate = 1Hz
NSLS-II BPM

- BNL in house designed/developed for NSLS-II project
- Very flexible environment for DSP/Firmware development
- Satisfied of all NSLS-II performance requirement

NSLS-II RF BPM (Production Unit)

Digital Front End (DFE)
ADC-Raw Data Measurement

Fill Patten Control for SR simulation

FFT
RF BPM Production - Test

RF BPM Laboratory Unit Test Setup (Bench #1)

- 500MHz MO
- Timing System
- Matlab – Generate test Report (15min test time)

Phase Noise Test Port @ ADC

- R&S FSUP8
- Matlab – Generate test Report (15min test time)
- Test Bench #2

Phase Noise (Jitter) Measurement

- 700fs (RMS)

BPM(1-8):
- Stability Test
  - 8hr Stability (um):
    - 0.3488
    - 0.2082
    - 0.1435
    - 0.1342
    - 0.1230
    - 0.1248
    - 0.1685
    - 0.1132

RF BPM Burn-In: “20-units” in Thermal Test Rack
Power Supply

Corrector Current control
# Summary Table – Storage Ring Power Supplies

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Qty</th>
<th>Max. Voltage</th>
<th>Max. Current</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main Dipole</strong></td>
<td>1</td>
<td>1200 V</td>
<td>450 A</td>
<td>Unipolar Switch-Mode, Digital Regulator center point tied to GND</td>
</tr>
<tr>
<td><strong>Quadrupole</strong></td>
<td>60</td>
<td>16 V</td>
<td>175 A</td>
<td>Unipolar Switch-Mode, Analog Curr. Regulator – 2 DCCTs</td>
</tr>
<tr>
<td>- A</td>
<td>120</td>
<td>22 V</td>
<td>175 A</td>
<td>1 PS per Magnet</td>
</tr>
<tr>
<td>- B</td>
<td>60</td>
<td>30 V</td>
<td>175 A</td>
<td>200 A</td>
</tr>
<tr>
<td>- C</td>
<td>60</td>
<td>30 V</td>
<td>200 A</td>
<td></td>
</tr>
<tr>
<td><strong>Sextupole</strong></td>
<td>40</td>
<td>40 V</td>
<td>120 A</td>
<td>Unipolar Switch-Mode, Analog Curr. Regulator- 'A' Per Magnet</td>
</tr>
<tr>
<td>- A</td>
<td>5</td>
<td>60 V</td>
<td>165 A</td>
<td>2 DCCTs</td>
</tr>
<tr>
<td>- B</td>
<td>12</td>
<td>16 V</td>
<td>120 A</td>
<td>Model A &amp; B = 1 PS per 6 Magnets Model C = 1 PS per 2 Magnets</td>
</tr>
<tr>
<td>- C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Global Horz. &amp; Vert. Correctors - A</strong></td>
<td>90</td>
<td>24 V</td>
<td>1.25 A</td>
<td>2 Channel Bipolar Linear, Analog Curr. Regulator - 4 Shunts</td>
</tr>
<tr>
<td><strong>Insertion Horz. Correctors - B</strong></td>
<td>12</td>
<td>30 V</td>
<td>30 A</td>
<td>Unipolar Switch-Mode, Analog Curr. Regulator – 2 DCCTs</td>
</tr>
<tr>
<td><strong>Skew Quad Corrector-C</strong></td>
<td>30</td>
<td>20 A</td>
<td>20 A</td>
<td>Bipolar Linear, Analog Curr. Regulator – 2 DCCTs</td>
</tr>
<tr>
<td><strong>Alignment Horz. &amp; Vert. Correctors - D</strong></td>
<td>180</td>
<td>25 V</td>
<td>22 A</td>
<td>2 Channel Bipolar Linear / Pre-Regulator, Analog Curr. Regulator - 4 DCCTs</td>
</tr>
<tr>
<td><strong>Dipole Trim – Corrector - E</strong></td>
<td>27</td>
<td>15V</td>
<td>4 A</td>
<td>2 Channel Bipolar Linear / Pre-Regulator, Analog Curr. Regulator – 4 DCCTs</td>
</tr>
<tr>
<td><strong>Dipole Trim – Corrector - F</strong></td>
<td>3</td>
<td>20 V</td>
<td>10 A</td>
<td>2 Channel Bipolar Linear / Pre-Regulator, Analog Curr. Regulator – 4 DCCTs</td>
</tr>
</tbody>
</table>

**Stability / Resolution: ppm of max I**
- DC 1 Quadrant

There is a total of 997 power supply channels used for the storage ring.

G. Ganetis
Cell Controller
Orbit Feedback Processor

• NSLS-II Orbit feedback processor is based on Xilinx Virtex6-240LX FPGA chip
• We can add custom functions for FOFB design
• Powerful DSP slice for parallel computing
• Easily implement gigabit communication (SDI, EVR)
• Integrate with embedded System (Microprocessor, DDR-3, Ethernet, UART...)
• Support model based high level design and low level logic design
FOFB Test Setup (32 Cell controller)

- Successfully tested 32 Cell controller communications
- BPM data used pattern generator
- 5 Gbps, 32 bit custom protocol data format
Cell Controller Unit

- 6.5 Gigabit/s SDI link for BPM data
- Gigabit Ethernet to EPICS IOC
- 100 Mbit/s link for corrector setpoints
- IO signals (16 inputs, 12 outputs, 4 Vout) for fast machine protection
- 2 GB DDR3 memory
- Virtex-6 FPGA
- DFE
- Embedded Event Received
- 6.5 Gigabit/s SDI link for BPM data
- RS232 for console
- Gigabit Ethernet to EPICS IOC
Digital Front End (DFE) Board

- Virtex-6 FPGA
- Embedded MicroBlaze soft core processor running TCP/IP lwIP stack in conjunction with EMAC Ethernet core
- 2 Gbyte DDR3 SO-DIMM
- 1 Gbps Ethernet
  - Hardware TEMAC
  - Memory throughput 6GBytes/sec
- (6) 6.5 Gbps SFP modules
- Fixed Point DSP Engine
- 1Gbit FLASH memory
- 4 Lemo differential output
- **Embedded Event Receiver**
  - Embedded EVR compatible with MRF’s event system
  - Very flexible and precise timestamp and time synchronization
Timing Synchronizations

- MRF’s EVG 230 – VME
- MRF’s EVR-VME, cPCI, PMC
- BPM – Embedded EVR
- CC – Embedded EVR
FOFB timing

First packet is local packet

Total processing time: 20 us

Dual Port RAM

To FOFB
SVD (Singular Value Decomposition)
Single cell (6*3) example

**SVD is most commonly used algorithm for fast and slow feedback**

**Already well proven algorithm during the many years**

- R: response matrix
  (matrix containing transfer matrix elements between corrector and BPM)
- M: number of BPM, N: number of corrector
- U: M*N orthogonal matrix (beam position vector)
- V: N*N orthogonal matrix (corrector strength vector)
- \( \Sigma \): diagonal matrix containing singular value of R
- \( R^{-1} \): inverse response matrix for calculate corrector strength value

\[ R^{-1} = V S^{-1} U^T \]

\[ \theta = R^{-1} X \]
Orbit feedback system architecture

Fast orbit feedback system algorithm (MIMO system)

\[ \ddot{d}_{gold} \]

\[ \text{Controller} \quad R^{-1} = \Sigma^{-1} U^T \]

\[ \text{Compensator} \quad (\text{PID etc}) \quad \tilde{\theta} \]

\[ \text{Accelerator} \quad R = \Sigma V^T \]

\[ R_{MxN} \bullet \theta_{Nx1} = d_{Mx1} \]

\[ \theta_{Nx1} = R^{-1}_{NxM} \bullet d_{Mx1} \]

R: response matrix

R^{-1}: reverse response matrix

FOFB baseline algorithm

Offline operation: kick each corrector \(\rightarrow\) measure all BPM and get response matrix R

\(\rightarrow\) calculate R^{-1} with SVD

(10KHz) operation: measure/distribute all BPM data \(\rightarrow\) calculate corrector setpoints

\(\rightarrow\) set correctors
Fast Orbit Feedback Algorithm – Implementation in FPGA

R^{-1} = V * 1/\sum * U^T

Use FPGA parallel computation features to implement the algorithm (assume 240 BPMs, 90 correctors)

U^T_1, U^T_2, ..., U^T_90 : input matrix vector -- download from control system as waveform PV

V_1, V_2, ..., V_90 : output matrix vector -- download from control system as waveform PV

Q_1(z), Q_2(z), ..., Q_90(z) : compensator for each eigenmode -- parameters download from control system
Sysgen model for single mode
Firmware Development

- Xilinx Embedded System Tool
- Model based digital signal processing
- HDL&C/C++ Mixed design
- PlaneAhead for system integration
FPGA partition for hardware timing optimization

Virtex-6 FPGA pin location

Xilinx Planeahed is a very powerful tool for development of the FPGA application
EPICS IOC

Waveform Out
- V 90*90*4 (32.4 kb)
- U 180*90*4 (64.8 kb)
- S^-1 90*4 (360 byte)
- P 90*4 (360 byte)
- I 90*4 (360 byte)
- D 90*4 (360 byte)

Waveform Input
- X,y 2*4*10k (80.0 kb)
- X,y 12*4*10k (480.0 kb)

AO
- P,I,D
- CC SDI control (32)

AI
- CC SDI status (32)
- BPM SDI status (32)

Mbbo
- CC Mask

Mbbi
- BPM Mask

Other record

Asyn Driver

TCP/IP Socket

Ethernet Driver

CAS
NSLS-II FOFB Status

- Conceptual design complete
  - Matlab/Simulink simulation and FPGA implementation
- Hardware production
  - Chassis and DFE completed (50 ea)
  - I/O board completed (50 ea)
  - BPM all unit production completed
- SDI (Cell node, BPM node) 5 Gbps communication test completed
- SDI for Power Supply 100 Mbps Control communication test completed
- Machine Protection is not yet implemented (Collection requirement..)
- BPM SDI integration test Completed
- Feedback algorithm simulation completed
- Last week started FOFB main project integrations
Development Schedule

- Integrate Feedback processing module in the main project (~Dec/2012)
- BPM side SDI integration (Oct, Nov/2012)
  - We tested pattern data for communication and we need test with real BPM data
- BPM and Cell controller communication test (~Nov/2012)
- EPICS IOC integration (~ Jan/2013)
- High level and Diagnostic software design (~2014)
- Commissioning of the Storage Ring (4/26/2012 ~ 9/13/2013)
  - FOFB system will be install 2/1/2013 ~
Summary

- Digital BPM system 33% (100) ready for Install and commissioning
- All Cell controller is ready for test and installation
- We implemented simple and Roberts protocol for global BPM data distribution
- We tested 32 remote cell communication link and BPM local link communication Both worked well
- Ready FOFB algorithm integration in to FPGA (Last week)
- We assume there are many technical issues for commissioning and operation
  - BPM/PS performance, FOFB Algorithm, Communication, Diagnostics But we have a lot of experience to solve that any problems
Acknowledgement

• BPM/ Cell controller development:
  Kurt Vetter (Diagnose Group)
  Joseph Mead (Instrumentation Group)
  Alfred Dellapenna (Diagnose Group)
  Marshall Maggipinto (Diagnose Group)
  Joseph De Long (Controls Group)
  Yuke Tian (Controls Group)
  Yong Hu (Controls Group)
  Om Singh (Diagnose Group)
  Bob Dalesio (Controls Group)

• PSC and PS design:
  Wing Louie (Power Supply Group)
  John Ricciardelli (Power Supply Group)
  George Ganetis (Power Supply Group)
Linac/LTB

BPM IOC (IBM server)

LtB (3), and LINAC (5) RF BPM Thermal Rack Installation

LtB (3) RF BPM

LINAC (5) RF BPM

M. Maggipinto
Top Model
ADC, TbT, FA (50 % Fill Pattern)
Single bunch Measurement

1st measured beam with RF BPM (LINAC BPM #1).

120pC Single-Bunch

“April 2, 2012”