PAUL SCHERRER INSTITUT

PSI

Roger Biffiger :: Software Engineer :: Paul Scherrer Institut

Embedded Event Receiver at PSI

180612 :: EPICS collaboration meeting :: Open Hardware Workshop

PSI – large research facilities has a new structure

- PSI
  - Large Research Facilities
    - Electronics and Control Systems
      - Digital Signal Processing
        - FPGA development
        - Embedded Software

PAUL SCHERRER INSTITUT

SwissFEL

1st phase 2013-16

Photocathode — Linear accelerators

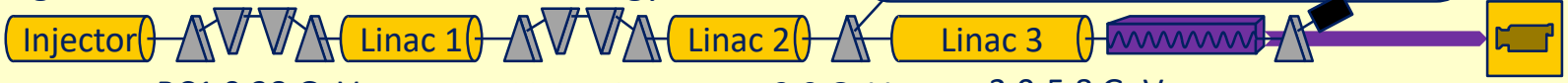
RF gun — C-Band technology

2nd phase 2018-19?

Athos 0.7-7nm

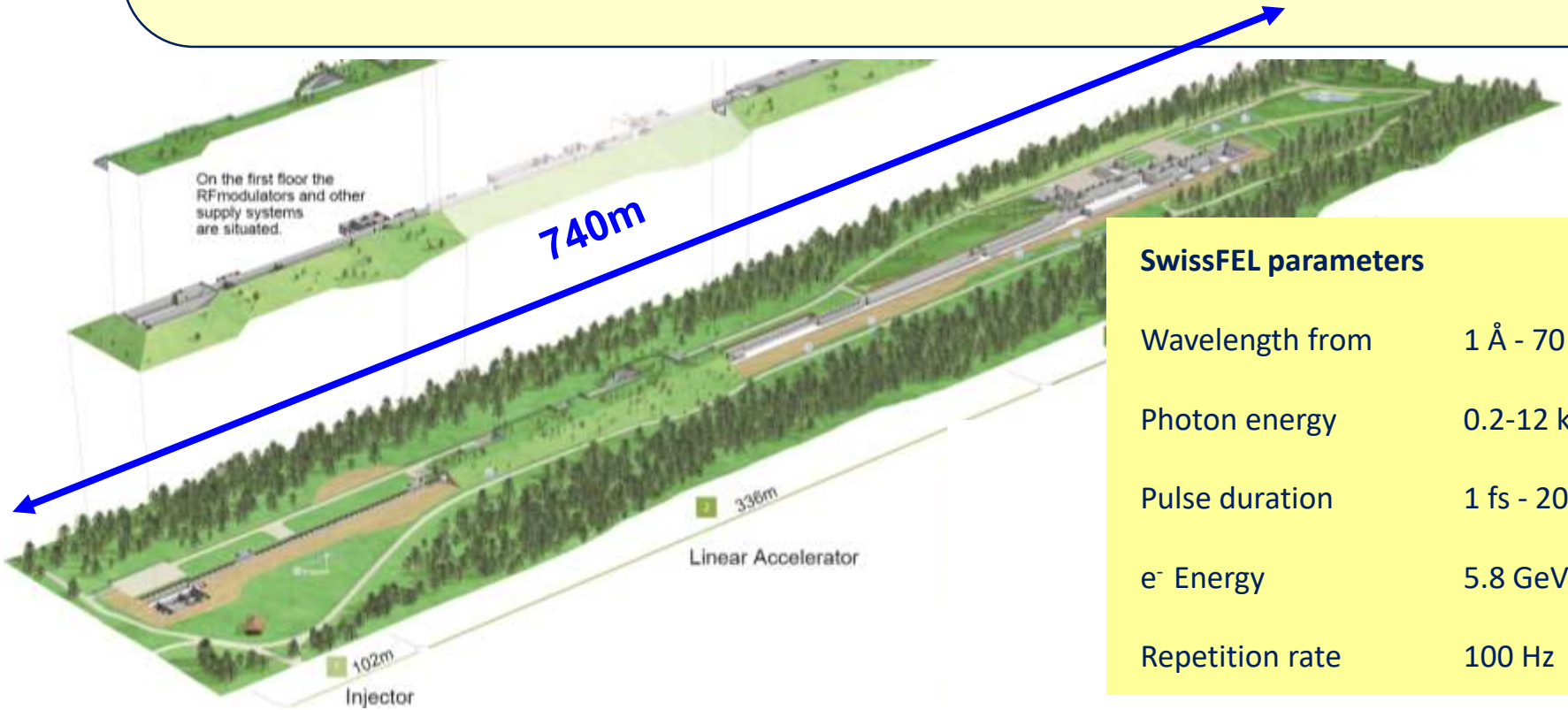
2.6-3.4 GeV

user stations



BC1 0.38 GeV — BC2 2.1 GeV — 3.0 GeV — 3.0-5.8 GeV

Aramis 0.1-0.7 nm



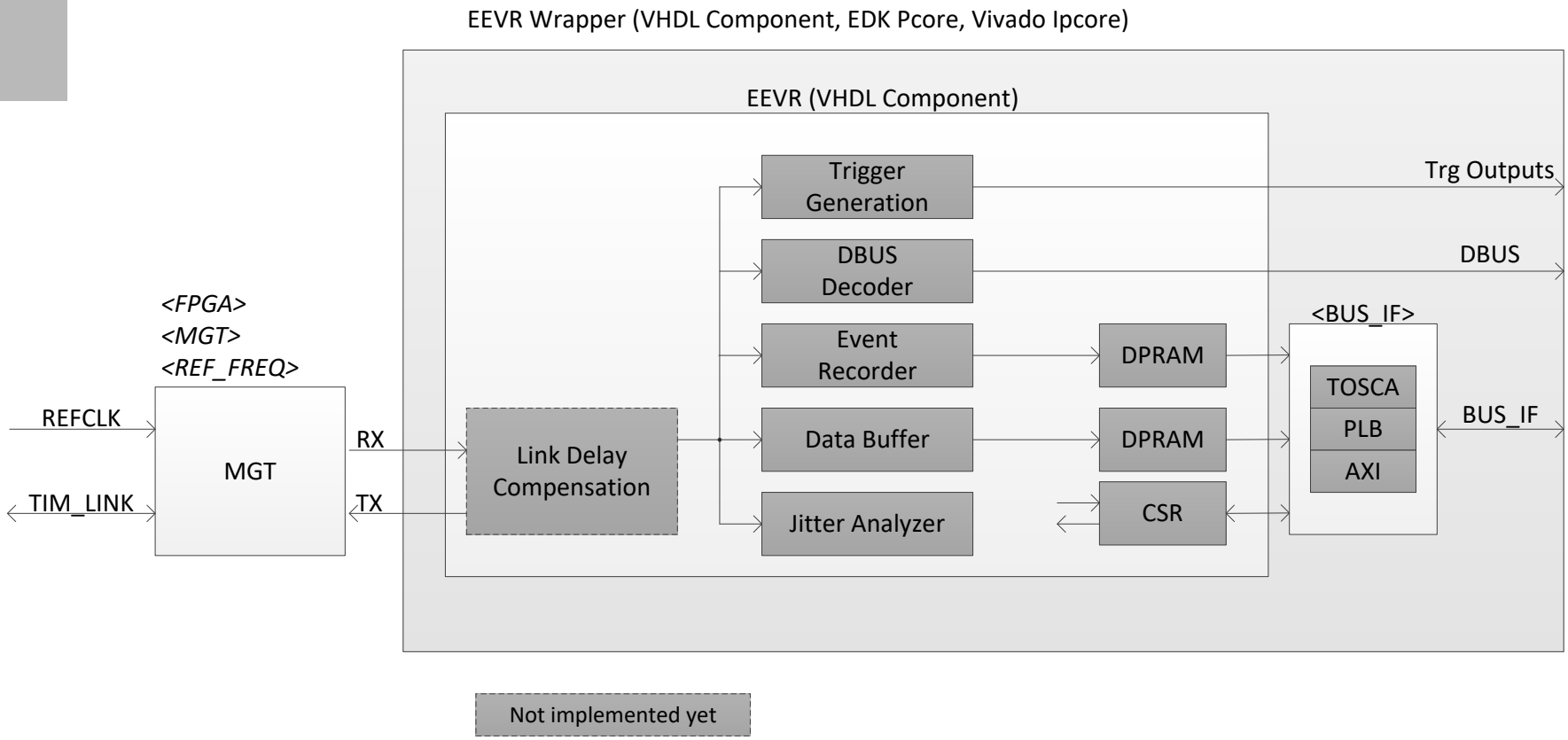
SwissFEL parameters

Wavelength from	1 Å - 70 Å
Photon energy	0.2-12 keV
Pulse duration	1 fs - 20 fs
e^- Energy	5.8 GeV
Repetition rate	100 Hz

EEVR at PSI

- EEVR functionality was developed in 2014 at PSI from protocol specification
- Motivation
  - Standalone systems without possibility of installing a hardware EVR.
  - Some systems needed only limited timing functionality. 1 or 2 triggers for the FW or SW and the data buffer containing the machine pulse id was sufficient.
  - Some applications need a specific functionality not provided in the standard EVR.
- Available as
  - VHDL component with TOSCA IF
  - EDK Pcore with PLB
  - Vivado IP Core with AXI Bus

EEVR current state



EEVR applications

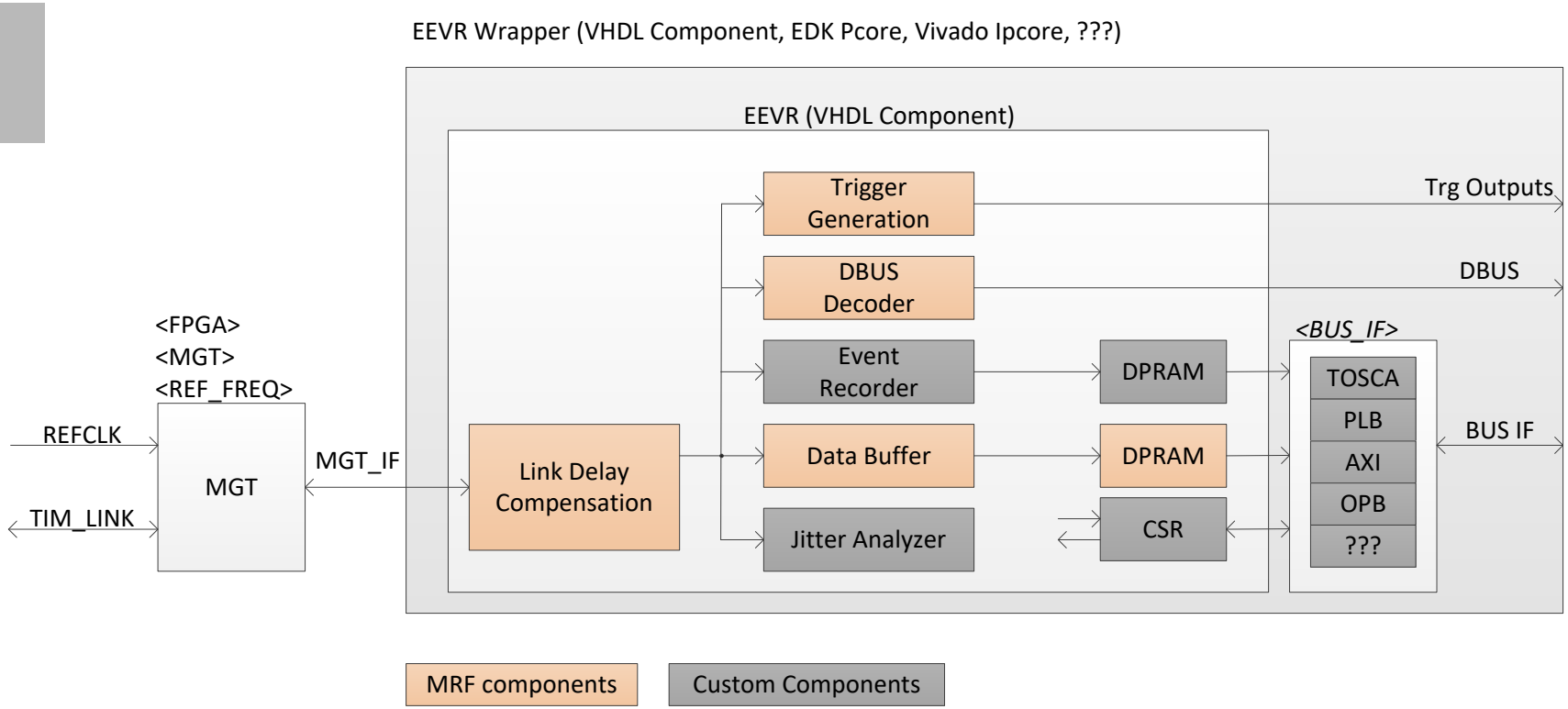
- The EEVR is used in various applications:
  - BPMs
  - LLRF system
  - photon diagnostics
  - experiments
- The EEVR is used on different HW boards:

Applications			
Board	**FPGA**	**MGT**	**BUS_IF**
IFC1210	Virtex-6	GTXE1	TOSCA II
GPAC2	Virtex-5	GTX_DUAL	PLB
GPAC3	Kintex-7	GTXE2	AXI
Eval Board	ZynqUltraScale+	GTH4	AXI
USI2 (planned)	Artix-7	GTPE2	AXI

Strategies for code reuse and collaboration

- Modular design
  - Source code for standard features provided by MRF
  - Source code for custom features provided by collaboration
  - Features selection by compilation parameters (generics)
- EEVR - common VHDL components for all applications
  - Wrappers are tool dependent and contain bus interfaces
- MGT is part of user application
  - MGT is FPGA dependent
  - MGT reference clock configuration is application dependent
  - Standardized interface between MGT and EEVR

Collaboration in action



My thanks go to

- Waldemar Koprek
- Patric Bucher
- Babak Kalantari