Table 33-14. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
B0	CLKOUT	t_{CYC}	12.5	—	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	10	—	ns
B1b	$\overline{BKPT}$ valid to CLKOUT high[3]	t_{BKVCH}	10	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{BKPT}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	6	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications have been indicated taking into account the full drive strength for the pads.
2 $\overline{TEA}$ and $\overline{TA}$ pins are being referred to as control inputs.
3 Refer to figure A-19.